

# IR-UWB Receiver Front-End for WSN Applications

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## Abstract

Ultra-wideband (UWB) has emerged as a very promising technology for short-range communication systems. The ultrashort duration of UWB waveforms gives rise to the potential ability to provide high-precision ranging and localization. Accurate distance measurements between sensor nodes used for localization in wireless sensor networks (WSNs) are very attractive for advanced wireless health-care applications. Over the years, several localization methods like received signal strength intensity (RSSI), angle of arrival (AoA) and time based approaches such as time-of-arrival (ToA) and time-difference-of-arrival (TDoA) exist for distance measurement between sensor nodes. The dominant RSSI is simply estimating the node distance by measuring the strength of the received signal. However, precision is too low with this method. ToA ranging approach is simple but require synchronization to give good precision. Clock synchronization between the transceivers is limiting the accuracy of the ToA estimation and hence increases the design challenges of the UWB ranging system. To our best knowledge no high-precision localization solution suitable for in-body tracking is reported.

Impulse radio ultra-wideband (IR-UWB) has been an interesting area of research for low-power short-range applications. Several studies indicate time-of-flight (ToF) measurements combined with the good temporal resolution of IR-UWB can give good precision. Typical distances between sensor nodes are in the order of ten meters that requires distance measurement is approximately one centimeter. Since radio waves propagate with approximately the speed of light, the time differences of less than 30 ps are required. With traditional clock driven circuit solutions, we need a clock rate of more than 30 GHz, which is not easy in standard technology. Using the new circuit solutions that are still in digital value but continuous in time (Continuous-Time Binary Value—CTBV), it is possible to find effective solutions for precise distance measurement in combination with communication, all are integrated on a single chip.

The main goal of this thesis is to develop an IR-UWB receiver front-end covering the frequency band of 3–5 GHz for the CTBV ranging system. The front-end consists of an antenna, a low noise amplifier, a band-pass filter, a downconversion quadrature mixer, a low-pass filter, a differential-to-single-ended converter and a continuous-time quantizer. These building blocks are assembled with other circuit elements of a functional impulse-based radio chip that is demonstrated at short distances. To reduce complexity and to minimize the power consumption, the proposed IR-UWB receiver front-end has been implemented as an energy threshold detector. The quantizer with tunable threshold acts as a single-bit ADC is implemented as a demodulation function. By avoiding using external components as well as high frequency sampling clock, the IR-UWB receiver front-end consumes less power and fully integrated is possible. The proposed IR-UWB receiver front-end is suitable for high-precision low-power low data-rate communication over a relative short range for WSN applications such as ranging and localization.



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# Chapter 1

## INTRODUCTION

### 1.1 Introduction to Ultra-Wideband

#### 1.1.1 UWB Overview

Historically, the concept of UWB was firstly developed in the early 1960s through research in time domain electromagnetics, where impulse measurement techniques were used to characterize the transient behaviour of a certain class of microwave networks. By the late 1990s, UWB technology had become more commercialized and its development had accelerated greatly. A substantial change occurred in February 2002, when the Federal Communications Commission (FCC) of the United States issued a ruling that UWB could be used for data communications as well as for radar and safety applications. Recently, UWB technology has received significant attention in both academic and industry for applications in consumer electronics and wireless communications. UWB has many benefits, including low power, high data rates, precise positioning capability, extremely low interference and availability of low-cost transceiver. UWB technology is different from conventional narrowband wireless transmission technology—instead of broadcasting on separate frequencies, UWB spreads signals across a very wide range of frequencies. Specifically, the FCC reserves the unlicensed frequency band between 3.1 GHz and 10.6 GHz for UWB wireless communication systems, with the power spectral density (PSD) satisfying a specific spectral mask. UWB devices can make use of an extremely wide spectrum of 7.5 GHz while not emitting enough energy to be noticed by narrower band devices nearby. This sharing of spectrum allows devices to obtain very high data throughput, but they must be within close proximity. The wide bandwidth and very low power make UWB transmissions appear as background noise.

#### 1.1.2 Definition of UWB

FCC rules provide the following definitions for UWB signaling [1]:

### Absolute Bandwidth

The UWB bandwidth is calculated as the difference between the upper frequency  $f_H$  of the -10 dB emission point and the lower frequency  $f_L$  of the -10 dB dB emission point.

$$B = f_H - f_L \quad (1.1)$$

### Center Frequency

The center frequency  $f_C$  is the average of  $f_H$  and  $f_L$ , that is,

$$f_C = \frac{f_H + f_L}{2} \quad (1.2)$$

### Fractional Bandwidth

The fractional bandwidth (FB) is defined as

$$FB = 2 \frac{f_H - f_L}{f_H + f_L} \quad (1.3)$$

According to the US FCC, a UWB system with  $f_C$  larger than 2.5 GHz must have an absolute bandwidth equal to or greater than 500 MHz, whereas, a UWB system with  $f_C$  smaller than 2.5 GHz must have a fractional bandwidth equal to or greater than 0.2.

## 1.1.3 UWB Spectral Masks

UWB systems cover a large spectrum and interfere with existing users. In order to keep this interference to a minimum, in 2002 the FCC and other regulatory groups specify spectral masks for different applications, which show the allowed power output for specific frequencies. UWB systems must transmit below certain power levels in order not to cause significant interference to the other systems in the same frequency spectrum. Fig. 1.1 and Fig. 1.2 illustrate the UWB spectral mask for indoor and outdoor communications under Part 15 of the FCC's rules [FCC02]. According to the spectral mask, the PSD of a UWB signal must not exceed -41.3 dBm/MHz for frequency ranges from 3.1 GHz to 10.6 GHz and it must be even lower outside this band, depending on the specific applications. In Europe, the recommendations for short-range devices belong to the European Conference of Postal and Telecommunications (CEPT) working group. The European Telecommunications Standards Institute (ETSI) participates in CEPT regulatory activities for harmonizing radio-communications in Europe. The European approach is somewhat different to the US regulatory approach, since it mandates more stringent power limits in the spectral mask. Generally, it is expected that ETSI/CEPT will follow the FCC's recommendations but will not necessarily directly adopt the FCC's regulations. In Japan and Korea, where UWB has been allowed but with different spectrum masks to those adopted in Europe and the US. These spectrum masks are "notched" to allow protection in particular bands between 3.1 GHz

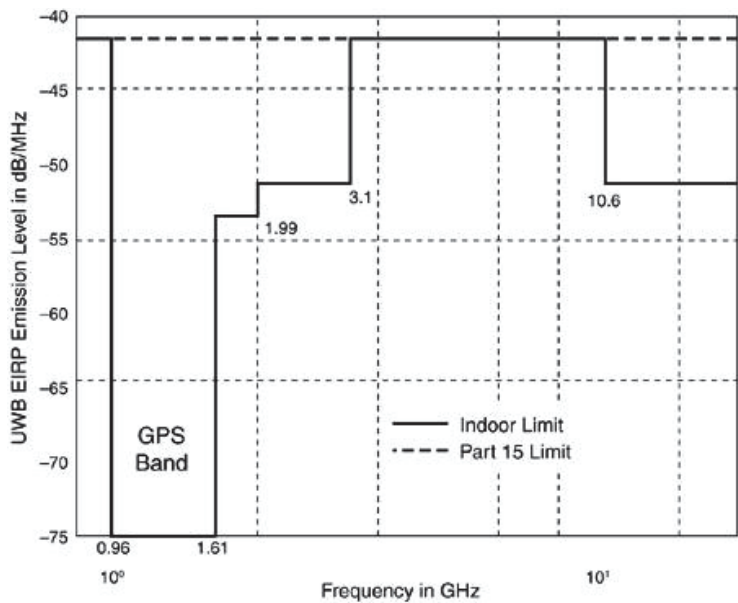


Figure 1.1: Spectral mask mandated by FCC 15.517 for indoor UWB systems.

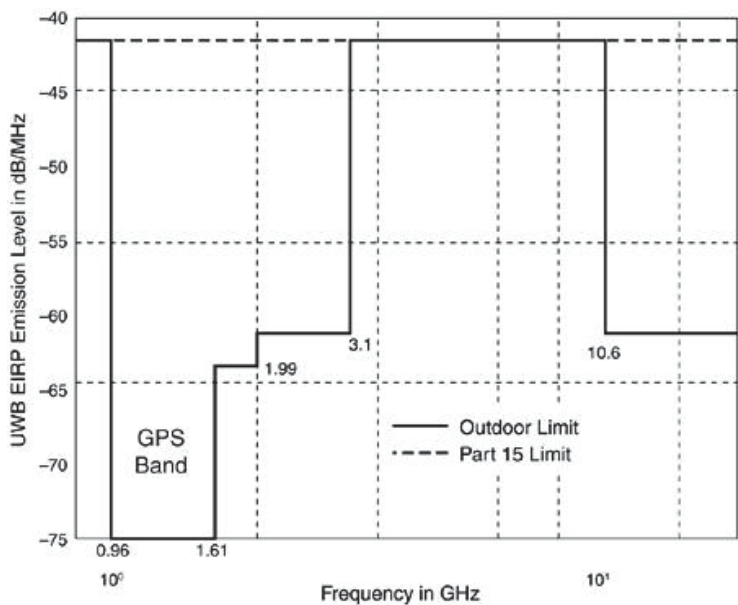
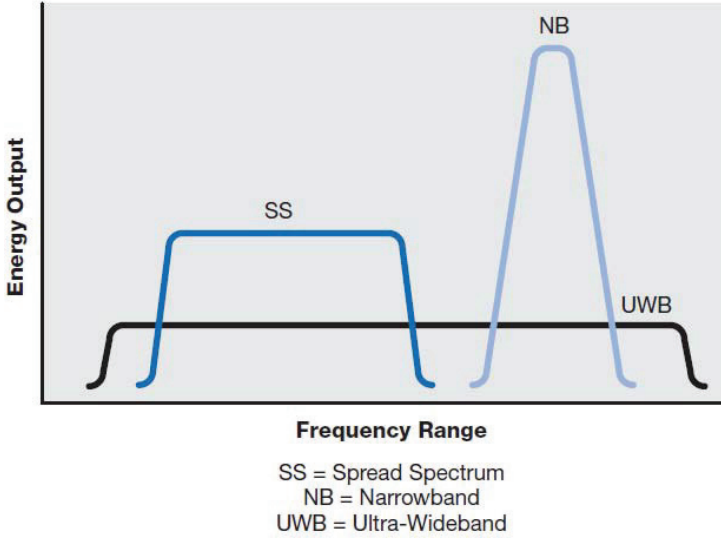


Figure 1.2: Spectral mask mandated by FCC 15.517 for outdoor UWB systems.



**Figure 1.3:** Comparison of NB, SS and UWB signal concepts [Intel].

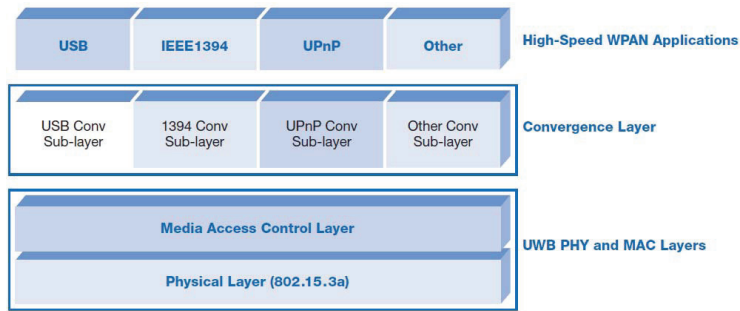
and 10.6 GHz. Other administrations such as Singapore and Hong Kong have allowed UWB trials in specific locations and have adopted similar masks to those implemented by Europe.

#### 1.1.4 Advantages of UWB

UWB differs substantially from conventional narrowband (NB) radio frequency and spread spectrum (SS) technologies. UWB uses an extremely wide band of RF spectrum to transmit data as plotted in Fig. 1.3. In so doing, UWB is able to transmit more data in a given period of time than the traditional technologies. The suitability of UWB signals for high-speed data communications can be observed from the Shannon capacity formula. For an additive white Gaussian noise (AWGN) channel with bandwidth of  $B$  Hz, the maximum data rate that can be acquired is given by

$$C = B \log_2(1 + SNR) \quad (1.4)$$

where  $C$  is the maximum channel capacity,  $B$  the signal bandwidth and  $SNR$  is the signal-to-noise ratio of the system. Shannon's equation suggests that there are three ways of improving the capacity of the channel: increasing the bandwidth, increasing the signal power or decreasing the noise. It also shows that the channel transmission rate grows linearly with channel bandwidth but only logarithmically with  $SNR$ . In other words, the channel capacity increases at a much faster rate with bandwidth than with power. Thus, UWB has the potential to offer very high data rates at low power consumptions. From the other point of view, the expansion of operating bandwidth allows a lower system  $SNR$  for the same capacity. As a result, UWB devices can have a much lower operating power than conventional narrowband communication systems. Low emission power is not only beneficial in power-constrained scenarios such as battery-operated devices, but also allows cheap RF components.



**Figure 1.4:** Applications and protocol layers for UWB [Intel].

UWB signals have low susceptibility to multipath interference occurred when a modulated signal arrives at a receiver from different paths. The ultrashort duration of UWB waveforms gives rise to a fine resolution of reflected pulses at the receiver. As a result, UWB transmissions is robust against multipath. Moreover, since UWB signals span a very wide frequency range, they show relatively low material penetration losses, giving rise to better link margins.

The carrier-free nature of the UWB signal transmission results in low complexity and low cost of UWB systems [2]. Unlike conventional radio systems, the UWB transmitter produces a very short time domain pulse which is able to propagate well without the need for additional upconversion and amplification. The very wideband nature of the UWB signal means it spans frequencies commonly used as carrier frequencies. The reverse process of downconversion may not required in the UWB receiver. Such an omission of upconversion/downconversion processes and RF components allows the entire UWB transceiver to be integrated into a single-chip, which contributes directly to low cost, small size and low power.

### 1.1.5 UWB Applications

With the characteristics of low power, low cost and very high data rates at limited range, UWB is firstly positioned to address the market for high-speed wireless personal area network (WPAN). Fig 1.4 represents the full solution stack required to make UWB a viable radio alternative in the marketplace. Intel Corporation has been working with the industry to develop protocols that will take full advantages of the strengths UWB technology [3]. The company envisions a future in which all devices are connected by smart radios. Many technologies used in the digital home, such as digital video and audio streaming, require high-bandwidth connections to communicate. Considering the number of devices used throughout the digital home, the bandwidth demand for wireless connectivity among these devices becomes very large indeed. The wireless networking technologies developed for wirelessly connecting PCs, such as Wi-Fi and Bluetooth Technology, are not optimized for multiple high-bandwidth usage models of the digital home. Although data rates can reach 54 Mbps for Wi-Fi, for example, the technology has limitations in a consumer electronics environment, including power consumption and bandwidth. When it comes to connecting multiple consumer electronics devices in a short-range network or WPAN, a wireless technology needs to support multiple high data rate streams, consume very

little power and maintain low cost while sometimes fitting into a very small physical package.

Alternatively, UWB transmission can trade a reduction in data rate for an increase in transmission range. Under the low-rate operation mode, UWB technology could be beneficial and potentially useful in WSN applications. The ultrashort duration of UWB waveforms makes them ideal candidates for high-precision ranging and localization [4]. A WSN comprises a large number of nodes spread over a geographical area to be monitored. If the time of flight of a pulse is known then it is possible to accurately estimate the distance travelled by the pulse from the source. By combining the distance estimated at multiple receivers, it is possible to use simple triangulation techniques to estimate the position of the source.

### 1.1.6 Challenges for UWB

UWB technology for short-range wireless communication has been pursued as a viable solution for high-speed communication. Along with many advantages, the UWB systems also bring in new challenges in implementation of the transceiver. Basically two approaches exist for exploring the largest unlicensed bandwidth ever released (FCC). Orthogonal frequency-division multiplexing (OFDM) is using several modulation carriers, each with more than 500 MHz bandwidth. In spite of significant research efforts, minor commercial successes are reported. An alternative UWB communication technology is use of pseudo-noise coded pulse sequences. Although potential large communication bandwidth may be feasible, the limited transmission power (part 15 limit) is degrading performance due to low SNR. Pursuing UWB solutions using standard system design, aiming for high communication bandwidth seem to be hard. However, exploring UWB solutions for alternative applications like short-range impulse radar or adding functionality like localization to short-range single-chip transceivers is only feasible with UWB technology. IR-UWB solutions in standard CMOS technology are hard to design and efficient single-chip systems may need a different design approach.

## 1.2 Main Contributions

Recently, UWB technology has been studied for ranging and localization in WSNs. The challenges of accurate distance measurement between sensor nodes are low power and minimal size. At the Nanoelectronics group, Department of Informatics, University of Oslo, we have brought forward a different way of designing IR-UWB based systems using Continuous-Time Binary-Value (CTBV) technique [5]. CTBV coding has been exploring in a power efficient IR-UWB ranging system that will be discuss in Chapter 2. The work in this thesis is a part of the IR-UWB CTBV ranging system. The main goal is to develop an IR-UWB receiver front-end covering the frequency band of 3–5 GHz. The proposed receiver front-end has been realized in 90 nm CMOS technology. 10 publications have been selected to be included in this thesis and can be summarized as follows

**Paper I:** "An Inductorless 3-5 GHz Band-Pass Filter with Tunable Center Frequency in 90 nm CMOS," The 2013 IEEE International Symposium on Circuits and Systems (ISCAS 2013).



An inductorless tunable switched-capacitor band-pass filter (BPF) based on N-path periodically time-variant networks is presented. The proposed UWB BPF is complete with ring-oscillator used for multi-phase clock generation suitable for power-efficient IR-UWB systems. The filter prototype was fabricated in TSMC 90 nm CMOS and occupies a chip area of 0.004 mm<sup>2</sup>. It archives a -3 dB bandwidth of 2 GHz while the center frequency can be tuned from 4 GHz to 4.4 GHz. Power consumption is 1.1 mW from a 1.2 V supply voltage. Noise figure (NF) is approximately 14 dB over 3–5 GHz bandwidth with minimal pulse dispersion. This filter is competitive to other start-of-the-art tunable BPFs and could substitute passive surface acoustic wave (SAW) filters for broadband wireless radio-communication.

**Paper II:** *"A 3-5 GHz IR-UWB Receiver Front-End for Wireless Sensor Networks,"* The 2013 IEEE International Symposium on Circuits and Systems (ISCAS 2013).

This paper presents an IR-UWB receiver front-end covering the frequency band of 3–5 GHz intended for low power, low data-rate communication over a relative short range for such applications like WSNs. The receiver front-end was designed and verified in 90 nm CMOS provided by TSMC. It employs direct-conversion (homodyne) architecture and occupies a chip area of 0.9 mm<sup>2</sup>. The front-end exhibits a peak gain of 45 dB at 4 GHz and consumes a total power of 26.6 mW from a 1.2 V supply voltage. Input return loss,  $S_{11} \leq -12$  dB and NF is between 8 dB and 9 dB through 3–5 GHz bandwidth.

**Paper III:** *"A Continuous-Time Differential Single-Bit Quantizer for IR-UWB Receivers,"* The 2013 IEEE International Conference on Ultra Wideband (ICUWB 2013), *accepted*.

In this paper, we propose a continuous-time differential single-bit quantizer intended for IR-UWB receivers. It exploits an active balun as the input to obtain single-ended to differential conversion. The quantizer prototype was fabricated in 90 nm CMOS and occupies a chip area of 0.09 mm<sup>2</sup>. The proposed quantizer achieves a -3 dB bandwidth covering the spectrum from 100 MHz to 2.5 GHz. The peak gain is 35 dB around 1 GHz and the sensitivity is 40 mV at 2 GHz. Power consumption is 13.1 mW from a 1.2 V supply voltage. The quantizer is compact and can be fully integrated without any external clock reference.

**Paper IV:** *"A Variable-Gain Single-Bit Ultra-Wideband Quantizer for Baseband Receiver Front-End,"* The 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2012).

This paper presents a variable-gain single-bit UWB quantizer suitable for baseband receiver front-end. The prototype chip is fabricated in 90 nm CMOS technology. The quantizer achieves a -3 dB bandwidth covering a spectrum from 10 MHz to 2.7 GHz. The overall gain can be varied from 23 dB to 33 dB while the NF is between 7 dB and 10 dB. The sensitivity is 40 mV at 2 GHz and 110 mV at 3 GHz. The quantizer core occupies a die area of 0.04 mm<sup>2</sup>. By avoiding high frequency sampling clock, power consumption is only 4.8 mW making the proposed quantizer suitable for low-power wireless communications.

**Paper V:** *"An Inductorless 6-Path Band-Pass Filter with Tunable Center Frequency for UWB Applications,"* The 2012 IEEE International Conference on Ultra Wideband (ICUWB 2012).

This paper presents an inductorless switched-capacitor 6-path BPF suitable for IR-UWB applications designed in nanometer CMOS technology. The proposed wideband BPF is working in discrete-time intended for power-efficient IR-UWB systems. As a part of the filter, a novel 6-phase clock generator is proposed enabling center-frequency tuning at microwave frequencies.

The 6-phase clock generator is built with digital logic gates, thus can be easily scaled to finer pitch technology. The BPF achieves a -3 dB bandwidth of 2.5 GHz with center frequency tuning range between 4.1 GHz and 4.5 GHz. The filter consumes a power of 4.5 mW from a 1.2 V supply voltage and occupies an area of 0.007 mm<sup>2</sup>. The filter is compact, suitable for standard digital technology and can be fully integrated without any external clock reference.

**Paper VI:** "*Continuous-Time High-Precision IR-UWB Ranging-System in 90 nm CMOS*," The 2012 IEEE Asian Solid-State Circuits Conference 2012 (A-SSCC 2012).

An IR-UWB communication solution with embedded ranging by measuring the symbol round trip time without a common reference clock is presented in this paper. A first working clockless IR-UWB ranging transceiver fabricated in 90 nm CMOS technology with fully integrated digital symbol detection including a running cross-correlator is implemented. The IR-UWB transceiver consumes a power of 5.6 mW from a 1.2 V supply voltage and occupies a chip area of 3.6 mm<sup>2</sup>. Preliminary measured results shows that two transceivers in a master-slave configuration can estimate distance with precision  $\approx 1.4$  cm. The IR-UWB ranging system is power and area efficient, giving superior ToF distance measurements which can be used for WSN applications.

**Paper VII:** "*An Ultra-Wideband, Continuous-Time, Differential, Single-Bit Quantizer in 90 nm CMOS*," The 54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2011).

In this paper, we propose a UWB, differential, single-bit quantizer intended for IR-UWB applications using standard 90 nm TSMC digital CMOS technology. The proposed quantizer is working in continuous-time for power-efficient IR-UWB implementations with a 5 GHz bandwidth and a very high differential gain of approximately 70 dB while consuming 33.5 mW from a 1.2 V supply voltage. A T-coil and a center-tap inductor are explored for bandwidth enhancement resulting in an bandwidth extension of 2.5 times compared to the uncompensated case.

**Paper VIII:** "*A 70-dB, 3.1-10.6-GHz CMOS Amplifier in Low-Power 90 nm CMOS*," The 54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2011).

The analysis, design and implementation of a high-gain UWB amplifier is proposed. It is the core of the 3.1-10.6-GHz quantizer introduced in [Paper IX] but this paper presents in detail several crucial characteristics of the novel UWB amplifier and it may find usage in other wideband applications. The amplifier is based on cascaded multistage resistive-feedback inverters with an input LC resonator for bandwidth extension. This is confirmed by post-layout simulation in a TSMC 90nm CMOS low-power process. Simulated results show that the amplifier exhibits a 70 dB gain throughout the bandwidth from 3.1 GHz to 10.6 GHz. The amplifier is area-efficient using only one inductor for bandwidth enhancement. It occupies an area of 0.95 mm<sup>2</sup> and consumes a power of 25.1 mW from a 1.2 V supply voltage.

**Paper IX:** "*Continuous-Time CMOS Quantizer for Ultra-Wideband Applications*," The 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010).

A continuous-time CMOS quantizer suitable for UWB single-bit quantization is presented in this paper. The proposed quantizer achieves a -3 dB bandwidth covering the entire FCC UWB spectrum from 3.1 GHz to 10.6 GHz with a very high gain of approximately 70 dB. Instead of using multiple peaking inductors for bandwidth enhancement, a resonant peak at the amplifier

corner frequency can 'pull up' the gain, thus extending the bandwidth significantly. In this design, only a single, small inductor (0.7 nH) is used regardless of the number of amplifier stages. The proposed quantizer occupies an area of 0.12 mm<sup>2</sup> and consumes a power of 25.5 mW from a 1.2 V supply voltage.

**Paper X:** "*UWB Vivaldi Antenna for Impulse Radio Beamforming*," The 27th Norchip conference (NORCHIP 2009).

In this paper, two different types of Vivaldi antenna are designed and tested on Rogers RO4350B substrate with a relative constant of 3.48, thickness of 1.52 mm and loss tangent of 0.0031. The first is an antipodal Vivaldi antenna and the other is a tapered slot Vivaldi antenna. They are both ultra wideband antennas for the 1–5 GHz frequency band with low impulse distortion and the voltage standing wave ratio (VSWR)  $\leq 2$  throughout the entire bandwidth.

## 1.3 Thesis Outline

The contents of the thesis can be divided into eight chapters. Summarized below are overviews of each chapter.

**Chapter 1:** The thesis starts with an introduction to the basic concepts of UWB technology in chapter 1. Advantages, applications and its challenges are also presented.

**Chapter 2:** Chapter 2 reviews conventional positioning techniques followed by the proposed architecture of the IR-UWB CTBV transceiver for high-precision ranging and localization.

**Chapter 3:** This chapter covers the design of switched-capacitor (SC) filters based on N-path periodically time-variant networks. Switched-capacitor techniques are the most common approach for realizing integrated filters due to their high degree of accuracy and linearity. The purpose of this chapter is to provide ideas and discussions for using SC N-path filters as BPFs and their realization in CMOS technology. In this chapter, an inductorless SC 5-path BPF implemented in TSMC 90 nm CMOS is demonstrated. The performance was verified by measurements. Besides, another 6-path BPF along with novel 6-phase clock generator is proposed and post-layout simulation results are given.

**Chapter 4:** Chapter 4 focuses on designing of UWB continuous-time single-bit quantizers in standard digital 90 nm CMOS technology. Four different architectures of quantizers are proposed including both single-ended and differential approaches. Two different quantizers were fabricated in TSMC 90 nm CMOS and extensive measurements have verified the performances of the proposed designs. Moreover, bandwidth enhancement techniques using peaking inductors are introduced to extend the quantizers' bandwidths towards high frequency suitable for FCC band. Comparisons to the state-of-the-art works are also provided to more clearly evaluate the proposed design.

**Chapter 5:** This chapter deals with low noise amplifiers and mixers which are important building blocks of communication systems. After giving a review of typical sources of noise, a variety of conventional LNA architectures are discussed in detail where matching and noise considerations are important issues. Advantages and limitations of each topology are also addressed following by a proposed solution for 3–5 GHz LNA. The latter section of this chapter

is devoted to provide an overview of active and passive mixers. A novel quadrature mixer is then proposed including a QVCO that can eliminate bi-modal oscillation. Finally, the chapter concludes with post-layout simulation results of proposed LNA and downconversion quadrature mixer.

**Chapter 6:** Beginning with brief definitions of antenna parameters and then concentrating on a particular type of UWB antenna, that is Vivaldi antenna. Two different UWB Vivaldi antennas were investigated and then fabricated on Rogers substrate. This chapter concludes with a comparison between tapered slot Vivaldi antenna and antipodal Vivaldi antenna.

**Chapter 7:** The object of this chapter is to propose an IR-UWB receiver front-end for CTBV ranging system. All the building blocks have been presented in the previous chapters are put in together in a single-chip solution.

**Chapter 8:** This chapter concludes the thesis and then presents the future research trajectory.

# Chapter 2

## UWB RANGING SYSTEMS

### 2.1 Introduction

Precision localization has been one of the fascinating application areas for IR-UWB technology. These applications exploit the fine time resolution of UWB signals. The ultrashort pulse waveform enables UWB receivers to accurately determine the time of flight (ToF) of the signal transmitted from another UWB transmitter. UWB technology is particularly well suited for WSN applications due to its low power consumption. Several reported systems for low data rates, low power and low complexity short-range communications and ranging have been demonstrated. Most IR-UWB designs focus on non-coherent receivers due to low complexity [6]- [10]. However, the non-coherent receivers show relatively poor performance in terms of ranging accuracy. In [6], a low-complexity non-coherent IR-UWB transceiver operated at 3.1–4.1 GHz frequency band, is presented. The transceiver exploits energy-collection-based TOA estimation for positioning. However, the positioning accuracy is  $\pm 5$  ns corresponding to 150 cm. In [10], a single-bit quantizer and auto-correlation followed by integration for pulse recovery is proposed. The actual time-of-arrival information is lost with the integration and limits the ranging accuracy to approximately 30 cm. An embedded ranging system for the ISM band is demonstrated in [11]. It combines the advantages of both broadband and narrowband signals to improve ranging accuracy. However the ranging accuracy is still around 20 cm. The accuracy is less than 15 cm in [12] demanding high speed ADCs. Others reported ranging solutions are limited by clock frequency or clock synchronization and hence increases the design challenges of the UWB ranging system. For example, 1 GHz clock can give rise to 30 cm precision with high design complexity, which is not sufficient. For ranging accuracy better than 1 cm, we need a clock exceeding 30 GHz, which is quite challenging with the current CMOS process technology.

At the Nanoelectronics group, Department of Informatics, University of Oslo, we have brought forward a different way of designing IR-UWB based systems named Continuous-Time Binary-Value (CTBV) using pure time-domain signal processing [5]. By avoiding clocks, power efficient solutions are feasible in standard CMOS. Although process variations pose significant challenges, high-speed and power-efficient CMOS implementations have been demonstrated [13] [14]. Our goal is to take the benefit of the wideband characteristics of impulse radio systems and seek a system solution which dramatically cuts down the implementation cost while exploring

the inherent capability of fine-timing resolution. Using a two-way ranging between the sensor nodes, the distance can be estimated by measuring the symbol round-trip time without a common reference clock [15]. The proposed CTBV ranging system in a master-slave configuration is employed to estimate ToF for high-precision localization with a reported ranging accuracy of  $\approx 1.4$  cm, data rate of 1.5 Mbps [Paper VI] [16]. This chapter first reviews conventional positioning techniques and then proposes a novel IR-UWB CTBV transceiver for high-precision ranging and localization.

## 2.2 Positioning Techniques

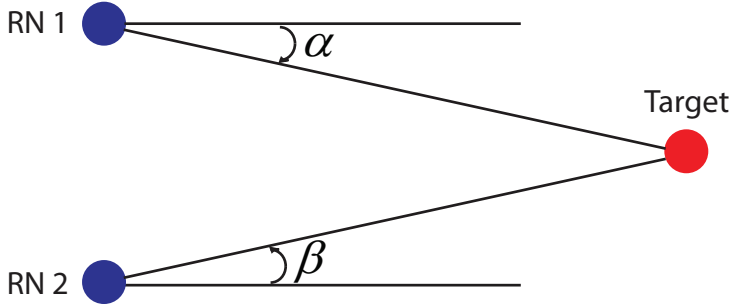
Positioning techniques exploit one or more characteristics of radio signals to estimate the position of their sources. Positioning techniques can be divided into three main categories: the received signal strength intensity (RSSI), the angle of arrival (AoA) and the time-based approaches such as the time of arrival (ToA) and the time different of arrival (TDoA). The AoA technique measures the angles between a given node and a number of reference nodes to estimate the location while the RSSI and time-based approaches estimate the distance between nodes by measuring the energy and the travel time of the received signal, respectively. This section aims to provide a brief introduction of these positioning/localization techniques [1] [4] [17].

### 2.2.1 Received Signal Strength Intensity

RSSI measurements provide information about the distance between two nodes based on certain channel characteristics. The main idea behind an RSSI-based approach is that if the relation between distance and power loss is known, the RSSI measurement at a node can be used to estimate the distance between that node and the transmitting node, assuming that the transmit power is known. The distance between two nodes provides a circle of uncertainty for the position of the target node. However, due to inaccuracies in both RSSI measurements and quantification of the distance versus path loss relation, distance estimates are subject to errors. Therefore, in reality, each RSSI measurement defines an uncertainty area instead of a circle. This distance-based technique requires at least three reference nodes to determine the two-dimensional location of a given node, using the well-known triangulation approach. Since the RSSI measurements depend on the channel characteristics, RSSI-based positioning algorithms are very sensitive to the estimation of channel parameters.

### 2.2.2 Angle of Arrival

Unlike an RSSI measurement that provides range information between two nodes, an AoA measurement provides information about the direction of an incoming signal. In this method, the angle of arrival of the signal sent by the target to be positioned is measured at several stationary reference nodes (RNs) by steering the main lobe of a directional antenna or an adaptive antenna array. Each measurement forms a radial line from the reference node to the target to be positioned. In two-dimensional positioning, the position of the target is defined at the intersection



**Figure 2.1:** AoA positioning principle

of two directional lines of bearing as depicted in Fig. 2.1. In practice, more than two reference nodes may be employed to combat inaccuracies introduced by multipath propagation effects. This method has the advantage of not requiring synchronization of the reference nodes nor an accurate timing reference. However, the AoA approach is not well suited to UWB positioning for following reasons. Due to the large bandwidth of a UWB signal, there is significant multipath time dispersion due to reflections from and diffraction around surrounding objects. As a result, the number of paths becomes very large, especially in indoor environments. Therefore, accurate angle estimation becomes very challenging with the existence of scattering from objects in the environment. Furthermore, the use of antenna arrays makes the system costly, suppressing the main advantage of a UWB radio equipped with low-cost transceivers.

Assuming that the coordinates are  $(0, 0)$  and  $(0, y_2)$  for the reference node 1 and reference node 2, respectively. Given  $\alpha$  and  $\beta$ , respectively, as the angles of arrival of the signal from the target at reference node 1 and reference node 2. We can define two straight lines by

$$y = \tan(\alpha)x \quad (2.1)$$

$$y = \tan(\beta)x + y_2 \quad (2.2)$$

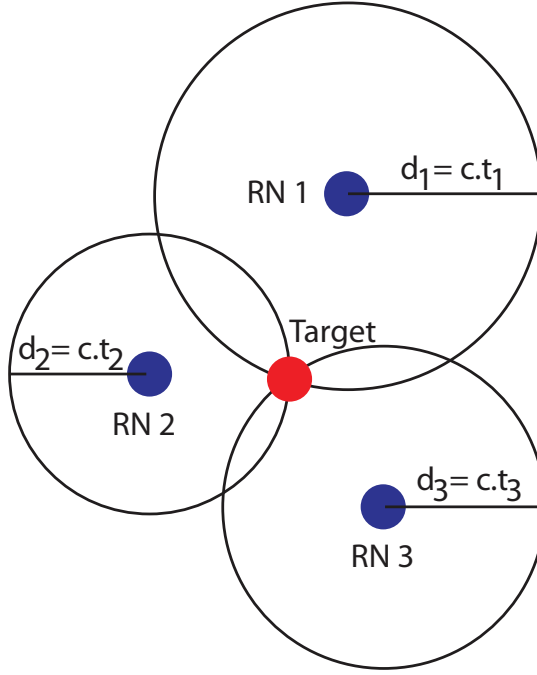
Substituting equation (2.1) into equation (2.2) yields

$$x = x_0 = \frac{y_2}{\tan(\alpha) - \tan(\beta)} \quad (2.3)$$

Substituting  $x_0$  into equation (2.1) gives a unique  $y_0$  and thus the point defined by the coordinates  $(x_0, y_0)$  is the target position.

### 2.2.3 Time of Arrival

ToA measurements provide information about the distance between two nodes by estimating the ToF of a signal that travels from one node to the other. Therefore, a ToA measurement at a node provides an uncertainty region in the shape of a circle. In two-dimensional positioning, at least three circles are required as shown in Fig. 2.2. Time-based schemes provide very good



**Figure 2.2:** ToA positioning principle.

accuracy due to the high time resolution of UWB signals. Moreover, they are less costly than the AoA-based schemes. Although it is easier to estimate RSSI than ToA, the range information obtained from RSSI measurements is very coarse compared with that obtained from the ToA measurements. However, the ToA technique requires knowledge of the transmission time of the emitted signal as well as synchronization of the target and reference nodes' clocks. Otherwise, large position errors can occur. For example, a clock inaccuracy of just 1 ns will lead to a position error of 30 cm. Furthermore, this technique can suffer from multipath propagation effects.

Assuming that the coordinates are  $(0, 0)$ ,  $(0, y_2)$  and  $(x_3, y_3)$  for the reference node 1, reference node 2 and reference node 3, respectively. Given that  $t_1$ ,  $t_2$  and  $t_3$  denote the time it takes the signal to travel from the target to be positioned to the respective reference nodes and  $c$  denotes the signal's speed of propagation, the distances between the target and each of the reference nodes are given by

$$d_1 = c.t_1 = \sqrt{x^2 + y^2} \quad (2.4)$$

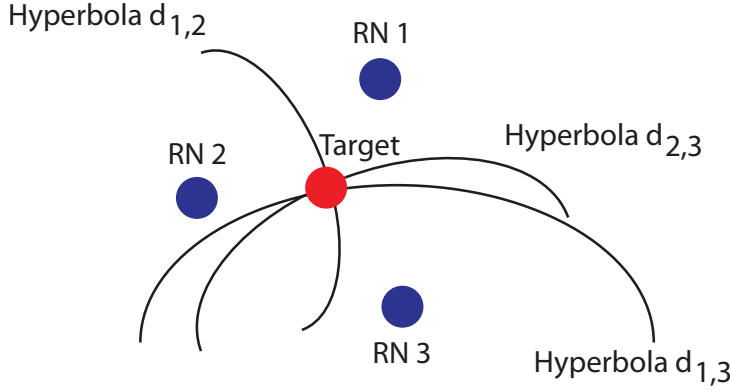
$$d_2 = c.t_2 = \sqrt{x^2 + (y - y_2)^2} \quad (2.5)$$

$$d_3 = c.t_3 = \sqrt{(x - x_3)^2 + (y - y_3)^2} \quad (2.6)$$

Each of these equations defines a circle whose  $x$  and  $y$  are unknowns. Squaring both sides of the above equations and some basic manipulation yields

$$y = y_0 = \frac{y_2^2 + d_1^2 - d_2^2}{2y_2} \quad (2.7)$$





**Figure 2.3:** TDoA positioning principle.

Substituting equation (2.7) into equation (2.4) gives two values for  $x$ . Only one of these values which is positive is correct.

## 2.2.4 Time Different of Arrival

In this technique, the difference between the arrival times of two signals traveling between the target node and the two reference nodes is measured. Each time difference is then converted into a hyperboloid with a constant distance difference between the two reference nodes. In two-dimensional positioning, at least two pairs of reference nodes are required. The position is the intersection of the two corresponding hyperboloids as depicted in Fig. 2.3. Conventionally, ToA-based range measurements require synchronization among the target and the reference nodes. However, TDoA measurements can be obtained even in the absence of synchronization between the target node and the reference nodes, if there is synchronization among the reference nodes. Here again, multipath propagation effects can affect the accuracy of the position and the location of the reference nodes.

Again, assuming that the coordinates are  $(0, 0)$ ,  $(0, y_2)$  and  $(x_3, y_3)$  for the reference node 1, reference node 2 and reference node 3, respectively. Given that  $t_1$ ,  $t_2$  and  $t_3$  denote the time it takes the signal to travel from the target to be positioned to the respective reference nodes and  $c$  denotes the signal's speed of propagation, the distances between the target and each of the reference nodes are given by

$$d_1 = c.t_1 \quad (2.8)$$

$$d_2 = c.t_2 \quad (2.9)$$

$$d_3 = c.t_3 \quad (2.10)$$

Defining two hyperboloids using the TDoA algorithm, that is

$$d_{1,2} = d_2 - d_1 = c.(t_2 - t_1) = \sqrt{x^2 + (y - y_2)^2} - \sqrt{x^2 + y^2} \quad (2.11)$$

$$d_{1,3} = d_3 - d_1 = c.(t_3 - t_1) = \sqrt{(x - x_3)^2 + (y - y_3)^2} - \sqrt{x^2 + y^2} \quad (2.12)$$

where  $x$  and  $y$  are unknowns. Taking the square in equations (2.11) and (2.12) yields

$$2d_{1,2}\sqrt{x^2 + y^2} = y_2^2 - d_{1,2}^2 - 2y_2y \quad (2.13)$$

$$2d_{1,3}\sqrt{x^2 + y^2} = x_3^2 + y_3^2 - d_{1,3}^2 - 2x_3x - 2y_3y \quad (2.14)$$

Equations (2.13) and (2.14) lead to

$$x = by + a \quad (2.15)$$

where  $a$  and  $b$  are calculated as

$$b = \frac{2y_2d_{1,3} - 2y_3d_{1,2}}{2x_3d_{1,2}} \quad (2.16)$$

$$a = \frac{x_3^2d_{1,2} + y_3^2d_{1,2} - y_2^2d_{1,3} + d_{1,2}^2d_{1,3} - d_{1,2}d_{1,3}^2}{2x_3d_{1,2}} \quad (2.17)$$

Substituting equation (2.15) into equation (2.13) gives

$$2d_{1,2}\sqrt{(b^2 + 1)y^2 + 2bay + a^2} = y_2^2 - d_{1,2}^2 - 2y_2y \quad (2.18)$$

This results in

$$[4d_{1,2}^2(b^2 + 1) - 4y_2^2]y^2 + [8bad_{1,2}^2 + 4(y_2^2 - d_{1,2}^2)y_2]y + [4a^2d_{1,2}^2 - (y_2^2 - d_{1,2}^2)^2] = 0 \quad (2.19)$$

Equation (2.19) is a quadratic equation with two roots that are the  $y$ -coordinates of the intersection points of the hyperboloids. Substituting the value of  $y$  into equation (2.15) provides the corresponding  $x$ -coordinates. To remove the ambiguity, we can define another hyperboloid by

$$d_{2,3} = d_3 - d_2 = c.(t_3 - t_2) = \sqrt{(x - x_3)^2 + (y - y_3)^2} - \sqrt{x^2 + (y - y_2)^2} \quad (2.20)$$

Substitution of  $d_{1,3}$  by  $d_{2,3}$  in equations (2.13)-(2.19) yields two points. One of these points matches the previous ones, which is the target position.

## 2.3 Proposed IR-UWB CTBV Ranging System

A different approach for IR-UWB radio named Continuous-Time Binary-Value (CTBV) signal processing has been proposed [5]. The idea is exploring ways to utilize the extremely fast computational speed of modern technology and improve the location functionality of wireless sensor networks. The CTBV technique is fundamentally a new approach to signal processing simply based on inherent CMOS process-dependent gate delays combined with a coarse quantizer or a single-bit analog-to-digital converter (ADC). In CTBV domain, the signal value is binary but time is kept continuous, which combines the speed of analog signal processing with some of the advanced processing capabilities of digital signal processing. An important property of the simple CTBV bit-stream is the accurate sampling time in principle eliminating quantization errors. As a result, the CTBV ranging system is very attractive for the emerging medical field such as wireless capsule endoscope which requires high accuracy localization and in-body communication. To our best knowledge no high-precision localization solution suitable for

in-body tracking is reported. Moreover, by avoiding clocks, power efficient solutions are feasible in standard CMOS while the performance of the CTBV solutions are only limited by the gate delays, thus can be scaled to finer pitch technology. We have been exploring CTBV coding in a power efficient IR-UWB transceiver for ranging system as proposed in Fig. 2.4. The chip prototype was fabricated in TSMC 90 nm CMOS and occupies a chip area of  $3.6 \text{ mm}^2$  as shown in Fig. 2.5. The key blocks of the ranging transceiver are: a quantizer, a continuous-time symbol detector, a symbol generator, a sequencer and a ranging and thresholding sampler doing the actual ToF measurement.

The basic principle to measure symbol round trip time using the CTBV ranging system can be explained as follows. In a master-slave configuration, the master is triggered to initiate a communication and the sequencer transmits a 32-bit symbol with a chip interval of 20 ns and starts the ranging circuit (sampler). To limit the hardware complexity, the symbol length is set to 32-bits, but is scalable to longer symbols for improved sensitivity. Gold code such as (1100001100100011100110110110101) is used for transmission, which has in-phase auto-correlation = 16, out-of-phase auto-correlation = 8 and cross-correlation = 8. Each pulse in the symbol is a fifth order Gaussian pulse filling a bandwidth from 3.1 GHz to 5.4 GHz [18]. The slave receives the symbol after some propagation delay and continuously looks for the expected symbol. The single-bit quantizer of the slave converts the incoming pulses into CTBV signals. Depending on where the threshold will hit the incoming signal, the quantized output may be very short pulses. Therefore, the output pulses from the quantizer are pulse extended by prolonging the rise time of the inverter with a weak PMOS. The RC time constant is tuned according to the desired pulse width and the pulse shape is recovered by a Schmitt trigger. Using a pulse extender, the pulse is reconstructed with sufficient pulse width to pass through the huge digital logic circuits in the following delayline without getting shrunk. In addition, the pulse width controllers in the delayline maintain pulse width throughout the delayline where the pulse can be either extended or shrunk.

The continuous-time symbol detector, presented in [19] [20], is composed of a delay line, a correlator, a counter and a match thresholder. The delayline consists of 31 delay elements to process the incoming 32-bit symbol. The cascaded delay elements provide a history of the incoming signal. Each delay element consists of coarse and fine tune. The pulse extended CTBV signal is stored in a delayline matching to the chip interval and is then cross-correlated in CTBV domain with a symbol template using a correlator based on simple AND gates. In CTBV coding, correlation refers to the matching of incoming '1's with the reference template. The correlated output are counted and coded as a thermometer coded digital value using the high speed counter. The counter output is then thresholded with an appropriate detection level using the match thresholder. The match thresholder consists of a multiplexer which is programmed through the SPI controller. Depending on the detected number of pulses in the incoming symbol, the appropriate threshold may be set [21]. If the incoming symbol matches the symbol template, the symbol pattern is detected. Immediately, the slave transmits another symbol pattern to the master and when the master receives this symbol in a similar procedure as the slave does, the ranging circuit in the master will have the symbol round-trip time (master-slave-master). The ranging circuit is a delay block continuously running to capture the symbol detected pulse in the sampler. The rise time of the symbol detected pulse in the sampler gives the measurement of

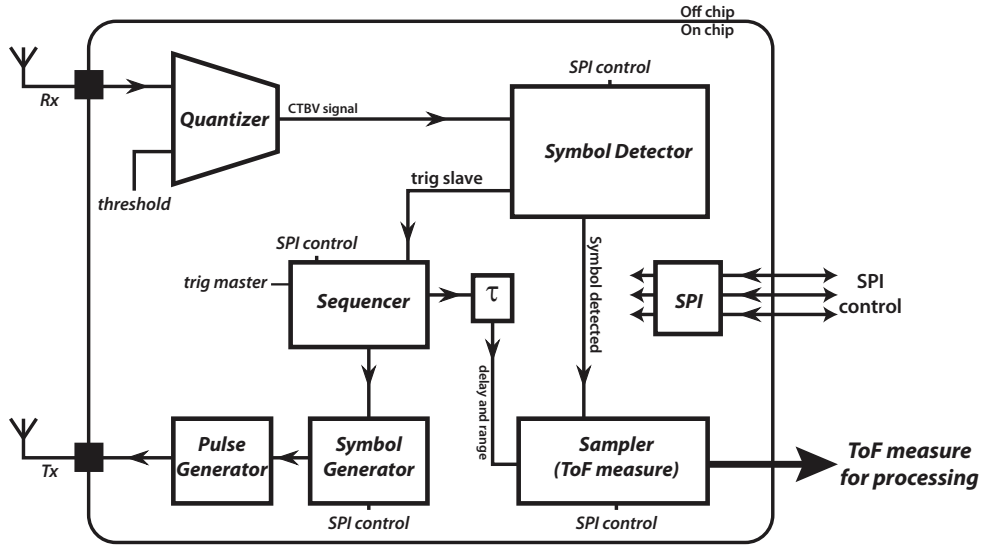
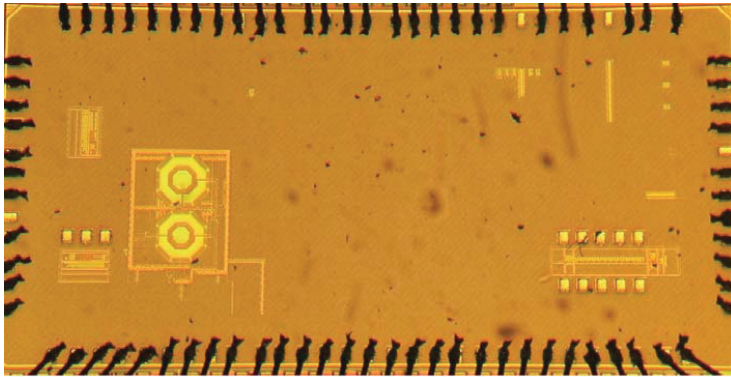
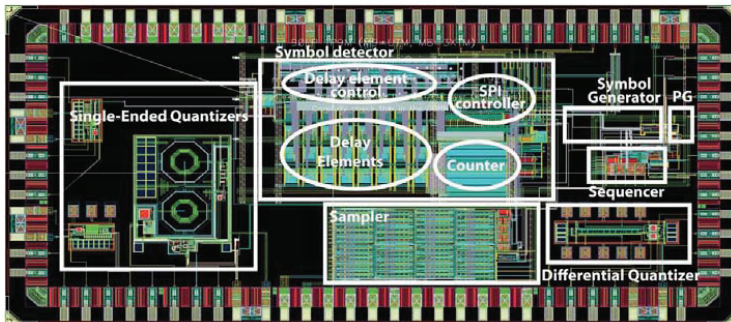


Figure 2.4: The proposed IR-UWB CTBV transceiver.

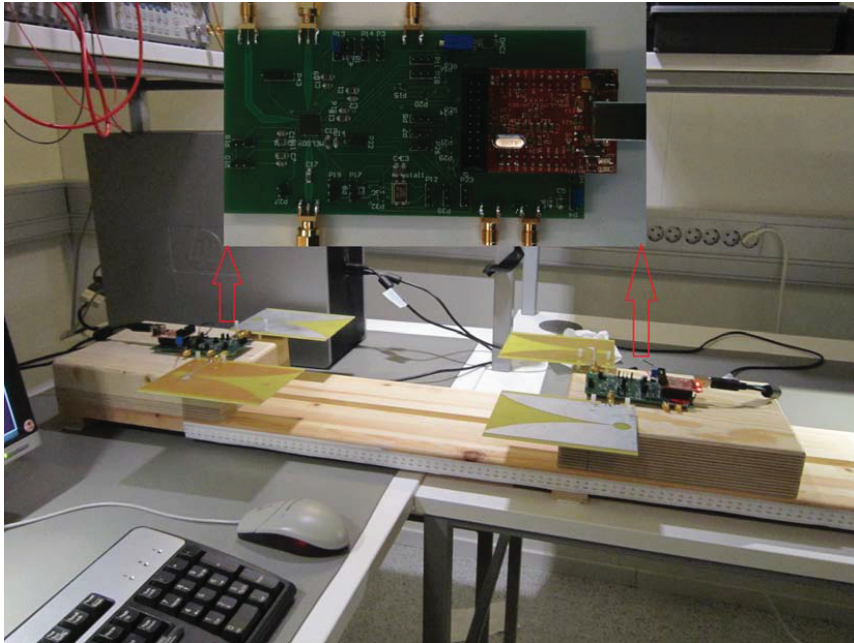


(a)



(b)

Figure 2.5: The chip microphotograph (a) and the layout (b) of the proposed IR-UWB CTBV transceiver.



**Figure 2.6:** The measurement setup for the IR-UWB CTBV ranging system.

total symbol round-trip time. The sampler consists of a delayline with 64 taps and 64 samplers (D flip-flops), each connected to a 16-bit counter. When the signal arrives, each of the taps on the delayline triggers the corresponding sampler and the counter is incremented. The unit delay in the sampler is around 100 ps, which limits the ranging accuracy in the current implementation but can be improved with technology scaling. Based on the symbol round-trip time, the ToF can be estimated precisely. Even in the absence of timing synchronization, the proposed transceiver does coherent symbol detection by preserving the timing information of the received symbol. The coherency of the symbol detection is obtained since cross-correlation is running in continuous-time and the detection pulse will be issued immediately when matching occurs. The complex power hungry synchronization circuits are completely avoided since continuous-time signal processing does not need clocks and also avoids aliasing and quantization noise [22] [23]. The symbol may be sent multiple times for improved symbol recovery, thus adding the processing gain. The process dependent variation, mismatch and jitter impacts the delayline where the delay element may cause variation both in the pulse position and also the pulse width of the incoming symbol, thus an initial calibration is required. The tuning or calibration procedure is done by programming each delay element to the required chip interval by coarse-tune and fine-tune register settings using a SPI interface to the microcontroller. The receiver are often called correlating receiver since template matching is required. Running cross-correlation is often power demanding. However, simple and power-efficient solutions are feasible using CTBV coding. The IR-UWB CTBV transceiver can be used as a ranging system for high-precision localization without any clock synchronization. The measurement setup for the IR-UWB CTBV ranging system is shown in Fig. 2.6.

A BER  $\approx 10^5$  is achieved for short range ( $<10$  cm). The BER rate can be improved further through several ways such as increasing the symbol length, symbol repetition, coding or including an IR-UWB receiver front-end. In this thesis, we propose an IR-UWB receiver front-end for improving BER as well as ranging accuracy. The front-end consists of an antenna, a low noise amplifier, a band-pass filter, a downconversion quadrature mixer, a low-pass filter, a differential-to-single-ended converter and a continuous-time quantizer. Each building block will be discussed in detail in the following chapters.

## 2.4 Conclusion

In this chapter, conventional positioning/localization techniques have been discussed. Due to the high time resolution of UWB signals, time-based location estimation schemes usually provide better accuracy than the others. Then we have presented a novel IR-UWB CTBV transceiver with embedded ranging by measuring the symbol round-trip time without a common reference clock. The IR-UWB transceiver was fabricated in TSMC 90 nm CMOS. It consumes a power of 5.6 mW from a 1.2 V supply voltage and occupies a chip area of  $3.6 \text{ mm}^2$ . Preliminary measured results shows that two transceivers in a master-slave configuration can estimate distance with precision  $\approx 1.4$  cm. Ranging resolution is not limited by the receiver complexity but limited by the available CMOS process technology. The IR-UWB ranging system is power and area efficient, giving superior ToF distance measurements which can be used for WSN applications such as high-precision ranging and localization.

# Chapter 3

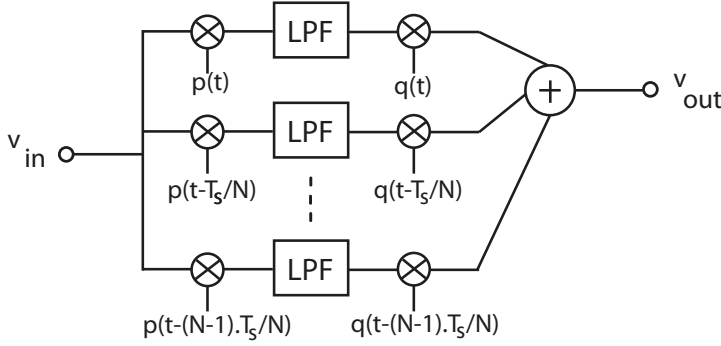
## UWB BAND-PASS FILTERS

### 3.1 Introduction

As wireless communication is moving up to higher frequencies, suitable integrated band-pass filters (BPFs) are required. Typically passive filters like surface acoustic wave (SAW) filters are used. Aiming at integrated filter solutions, SAW-filters are not viable [24]. An additional challenge is wideband, microwave filters for impulse radio applications. At microwave frequencies, wideband resonator based filters are hard to make and area consuming. There are various filter types that are appropriate for the implementation of RF on-chip BPFs include bulk acoustic wave (BAW) filters, active-RC filters, LC filters—often with Q-enhancement techniques,  $g_m$ -C filters and N-path filters. Unlike SAW filters, BAW filters are process compatible with silicon technology. However, their center frequency is sensitive to thickness variation of the piezoelectric material and the achievable tunability is limited. Although high linearity is an advantage of active-RC filters, these filters have a drawback of operating at high frequency ranges due to the limitation of the unity bandwidth of the operational amplifiers. Besides, it is not easy to implement tuning scheme. Q-enhancement approach has several disadvantages such as large area due to inductors which do not obey process scaling, limited tunability and poor dynamic range. Whereas, main drawbacks of  $g_m$ -C filters are the trade-off between power consumption, quality factor, center frequency and dynamic range and the need for tuning circuitry [25].

Recently, there has been a renewed interest in switched-capacitor (SC) N-path filters due to the development of CMOS technology allowing this type of filter to work at RF frequencies [26] [27]. They are also known as sampled data filters, commutated capacitors, etc. These filters basically transfer the low-pass/notch characteristic of a network to a band-pass/band-stop one by means of frequency mixers. An N-path filter can realize an inductorless tunable band-pass or band-stop filter in which the center frequency is determined by the mixing frequency. They have been widely utilized in receivers to replace SAW filters in low-cost wireless radio-communication applications. In addition to cost implications, these SAW filters not only degrade the receiver sensitivity due to their inevitable insertion loss, they are also hard to make tunable. Furthermore, the demand for fully integrated systems is favouring solutions with no external components achievable with novel receiver architectures as well as novel circuit topologies. SC circuits achieve high transfer-function accuracy with low distortion in CMOS technology and thus





**Figure 3.1:** The structure of an N-path filter.

become attractive for low-voltage operation. A combination of SC filter and N-path technique allows realization of high-quality RF filters even with simple ring-oscillators as multiphase clock generators. Still a major challenge is to generate a high-speed multiphase clock suitable for microwave filtering.

This chapter presents solutions for SC N-path BPF designed in nanometer CMOS technology [Paper I][Paper V]. The proposed wideband BPFs are working in discrete-time intended for power-efficient IR-UWB systems.

## 3.2 Principles of SC N-Path Filters

A typical N-path filter is composed of N parallel identical filter cells which are cyclically sampled with the frequency  $F_s$ . Each path usually in turn consists of a passive low-pass filter (LPF) with transfer function  $H(f)$  between an input and output mixer as shown in Fig. 3.1. The switches are driven by time/phase shifted versions of clock  $p(t)$  and  $q(t)$ . The time shift between two successive paths is  $T_s/N$ , where  $T_s$  is the period of the mixer clock. At any moment one and only one path is connected to the output node. When the switching signals are assumed to be ideal Dirac impulses delayed by  $T_s/N$ , the output signal  $S(f)$  may be written as a function of the input signal  $E(f)$  as shown in equation (3.1).

$$S(f) = \sum_{m=-\infty}^{+\infty} h(m \cdot T_s) \cdot \exp(-2 \cdot \pi \cdot j \cdot f \cdot m \cdot T_s) \cdot \sum_{n=-\infty}^{+\infty} e\left(\frac{n \cdot T_s}{N}\right) \cdot \exp(-2 \cdot \pi \cdot j \cdot f \cdot \frac{n \cdot T_s}{N}) \quad (3.1)$$

Equation (3.1) shows that the output signal is the result of two multiplied sums. The first term corresponds to the Fourier transform of the impulse response of the LPF sampled at  $T_s$  period. The second one corresponds to the Fourier transform of the input signal sampled at  $T_s/N$  period. Due to the periodicity of the frequency response, the band-pass center frequency is equal



to a multiple of the clock frequency. This filter can be used for clock recovery by filtering the harmonic components [28]. It can also be used as BPF centered around  $F_s$  [24]. Thus, the N-path filter transfers a low-pass characteristic to a band-pass whose center frequency is controlled by the clock frequency while the LPF and duty cycle of the clock define the bandwidth. In fact, the input signal is downconverted to baseband, filtered and then upconverted again to the same band as the input signal. Due to the Nyquist theorem, sampled-data filters can only process input signals up to half of the clock frequency. Since the transfer characteristic is the same for every switch position, the overall frequency response is equal to the response of an individual path. However, the output signal is now composed of N samples per period  $T_s$ , so that the Nyquist range NY for the N-path filter is expanded N times as follow

$$NY = N \cdot \frac{1}{2} \cdot F_s \quad (3.2)$$

The decomposition of filter center frequency and the filter properties is promising. A multiphase clock generator with wide tuning-range is required for center frequency tuning. The filter sharpness is determined by the sharpness of the LPF. For most wideband filters that do not require very high selectivities, a second-order passive LPF is sufficient.

A dominating error-source is clock feed-through due to the parasitic capacitors. This clock feed-through distortion produces not only an undesirable offset voltage but also additional spectral components at harmonics of the clock frequency  $F_s$ . These spectral components reduce the maximum dynamic range in the filter passband at  $F_s$ . Although even harmonics may be eliminated by using differential signaling [27], the clock feed-through is still a major challenge in designing SC N-path BPFs. In addition, due to tolerances in the filter paths, unwanted mirror frequencies can appear at the output [29].

### 3.3 Proposed UWB SC 5-Path Band-Pass Filter

#### 3.3.1 Low-Pass Filter

As mentioned before, the order and the corner frequency of the low-pass filter defines the roll-off and bandwidth of the N-path band-pass filter. A second-order RC LPF is designed for improved frequency roll-off as shown in Fig. 3.2. Thus, the gain decreases by 40 dB per decade above cut-off frequency. The frequency response of the second-order passive LPF is given in equation (3.3). Besides, the RC in each path of an N-path filter performs integration on the input signal when the corresponding switch is on. Any variation of R and C will result in filter bandwidth deviations from the designed value.

$$\frac{v_{out}}{v_{in}} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \left( \frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1}{R_2 C_2} \right) + \frac{1}{R_1 R_2 C_1 C_2}} \quad (3.3)$$

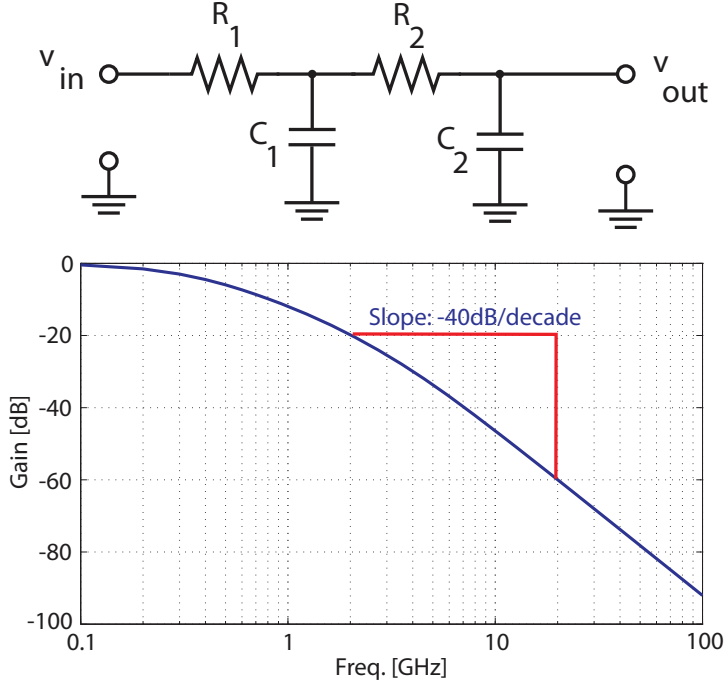


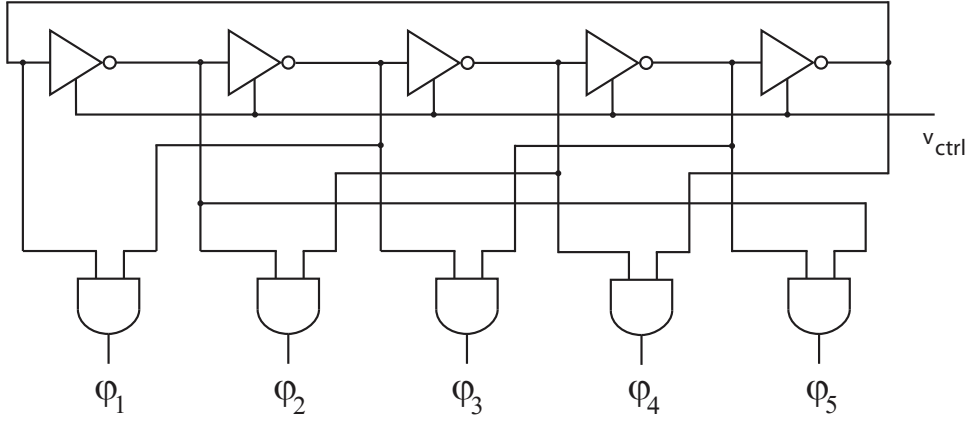
Figure 3.2: A second-order passive LPF and its frequency response.

### 3.3.2 5-Phase Clock Generator

Since the center frequency of the SC N-path BPF can be tuned with the clock frequency, a high-speed tunable oscillator is desirable. The tunability is particularly useful for RF integrated circuits, for which the tuning of the center frequency by a clock signal permits either to compensate for process variations and device mismatch or to filter various channels with the same filter. Several clock generator topologies for RF frequencies have been proposed in literature [30]. Most of them use inductors and capacitors to provide oscillation. These inductors occupy a very large area in the layout and are hard to adapt to finer pitch technology. In this design, a ring voltage-controlled oscillator (RVCO) based, multiphase clock generator is proposed in Fig. 3.3. Five inverters form a closed loop with positive feedback. It generates a 5-phase clock signal used for driving SC circuits. Avoiding an external crystal-driven clock, higher frequencies are feasible and full integration is possible. The 5-phase clock generator is built with digital logic gates and can be scaled with CMOS technology. The intrinsic propagation delays of each inverter are

$$t_{\text{PHL-INV}} = 0.7R_N C_L \quad (3.4)$$

$$t_{\text{PLH-INV}} = 0.7R_P C_L \quad (3.5)$$



**Figure 3.3:** The proposed 5-phase clock generator.

The oscillation frequency,  $f_0$  is given by

$$f_0 = \frac{1}{5(t_{\text{PHL-INV}} + t_{\text{PLH-INV}})} \quad (3.6)$$

where  $t_{\text{PHL-INV}}$  and  $t_{\text{PLH-INV}}$  are the high-to-low and low-to-high delay of the inverter,  $R_N$  and  $R_P$  are the equivalent resistances of the NMOS transistor and PMOS transistor, respectively and  $C_L$  is the load capacitance on the output of each inverter.  $C_L$  consists of the total gate capacitance from two transistors, the total drain capacitance from two transistors, routing capacitance and a possible additional capacitance or varactor. The delay in the inverter exists due to the time it takes the transistors in the inverter to charge  $C_L$ . If  $N$  is large enough, all nodes will be completely charged and discharged during one period and each inverter delivers the charge  $C_L V_{DD}$ . The transistor charging the capacitance will initially charge it with a maximum current  $I_D$ . The current decreases during the transition and if  $\eta I_D$  is the mean current (disregarding leak currents), the frequency of the RVCO is given by

$$f_0 = \eta \frac{I_D}{10 C_L V_{DD}} \quad (3.7)$$

where  $\eta$  is current ideality factor. According to equation (3.7), it is clear that  $f_0$  can be controlled through  $C_L$ ,  $V_{DD}$  and  $I_D$ .  $C_L$  can be controlled by a varactor, such as a biased PN junction. This is simple and effective, but also highly nonlinear [31]. A linear conversion can be obtained by switching on and off fixed capacitors, according to the magnitude of the input voltage. However, this requires large capacitor arrays at each node and, more importantly, an A/D converter is required to control the switches. Controlling  $V_{DD}$  will also influence  $I_D$ , as it is seen in the following sections. This principle has been shown to produce a reasonably good linearity. However, it requires high input voltages and the input signal is loaded with pulses and a generally low impedance. This solution is not suitable in a low supply voltage and low power circuit.  $I_D$  can be controlled through different current starving techniques. This approach results in a wide tuning range, but is also very nonlinear. Controlling  $I_D$  with the threshold voltage of

the transistors through the back-gate (bulk) voltage yields a better linearity. Furthermore, this solution implies a high and stable input impedance and if  $V_{DD}$  is lower than one diode voltage, it is possible to have rail to rail inputs or even input voltages exceeding the supply voltage. The behavior of the RVCO depends on the operation region of the transistors.

In strong inversion, the saturation drain current is given by

$$I_D = \frac{W}{2L} \mu_{\text{eff}} C_{\text{ox}} (V_{GS} - V_{th})^2 \quad (3.8)$$

where  $W$  and  $L$  are transistor dimensions,  $\mu_{\text{eff}}$  is the effective carrier mobility and  $C_{\text{ox}}$  is the oxide capacitance. When the bulk source voltage,  $V_{BS}$  is increased, the depletion area and thus the space charge is reduced. Due to charge neutrality through the MOS structure, the threshold voltage will be reduced according to

$$V_{th} = V_{t0} + \gamma \left( \sqrt{2\Phi_f - V_{BS}} - \sqrt{2\Phi_f} \right) - K_B V_{BS} \quad (3.9)$$

where  $V_{t0}$  is  $V_{th}$  when  $V_{BS} = 0$ ,  $\gamma$  is a process constant and  $\Phi_f$  is the surface potential of the MOS transistor. The first-order approximation of the current can be written as

$$I_D = \frac{W}{2L} \mu_{\text{eff}} C_{\text{ox}} (V_{DD}^2 + K_{\Phi}^2 - 2V_{DD}K_{\Phi} + \gamma^2 y^2 - 2\gamma(V_{DD} - K_{\Phi})y) \quad (3.10)$$

where  $K_{\Phi} = V_{t0} - \gamma\sqrt{2\Phi_f}$  and  $y = \gamma\sqrt{2\Phi_f - V_{BS}}$ . When  $V_{DD}$  is high, the linear dependency on  $y$  is dominating and the current will grow with a power to  $V_{BS}$  larger than one. When  $V_{DD}$  is reduced, the linear second-order effect in equation (3.9) becomes more important, making the dependency more linear.

In weak inversion, according to [32], the drain current can be calculated as

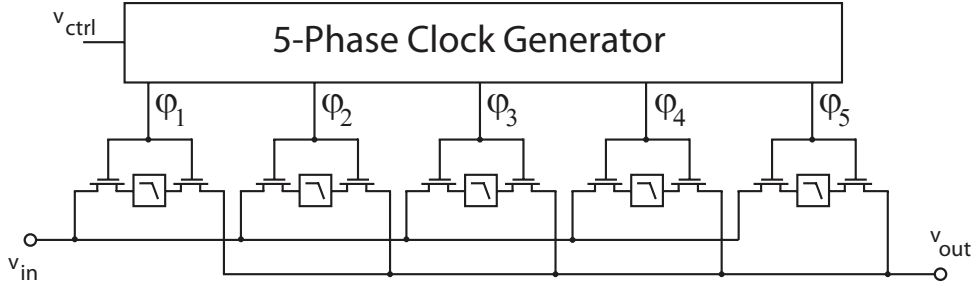
$$I_D = \frac{kT}{q} D \frac{W}{L} C_{\text{ox}} e^{\frac{q(V_{GS} - V_{th})}{\eta kT}} \left[ 1 - e^{\frac{-qV_{DS}}{kT}} \right] \quad (3.11)$$

where  $D$  is the diffusion coefficient of the carriers. The threshold voltage  $V_{th}$  given by equation (3.9) is independent of the operation region of the transistor. This means that the maximum current and thus the frequency in weak inversion, is proportional to

$$I_D \propto e^{-\gamma\sqrt{2\Phi_f - V_{BS}}/nV_T} \quad (3.12)$$

This implies that  $I_D$  is a function of  $V_{BS}$  to a power higher than one and the sensitivity of the RVCO will be increased with  $V_{BS}$ . In order to tune the oscillation frequency, both bulk voltages of NMOS transistor and PMOS transistor can be controlled. However, it would require two different voltage levels dependent on each other which is difficult to accomplish. Therefore, in this design, we only change the bulk voltage of the PMOS devices of the inverters in the ring.

The main drawback of this multiphase clock generator is relatively high phase noise level of the inherent ring oscillator compared to that of the LC oscillator. The phase noise of the ring



**Figure 3.4:** The proposed UWB SC 5-path BPF.

oscillator is investigated in [33], an can be calculated as

$$L(\Delta\omega) = A_k \frac{kTR_{ns}}{V_A^2} \left( \frac{w_0}{\Delta\omega} \right)^2 \quad (3.13)$$

where  $A_k$  is a factor depending on the noise generation mechanism studied,  $k$  is the Boltzmann's constant,  $T$  is the temperature in Kelvin,  $R_{ns}$  is an equivalent noisy resistor,  $V_A$  is the voltage amplitude of the signal and  $\Delta\omega$  is the frequency offset. In order to reduce the phase noise, the equivalent resistance  $R_{ns}$  must be reduced trading off against increase in power consumption.

### 3.3.3 Proposed Band-Pass Filter

Fig. 3.4 shows the proposed SC 5-path BPF. It consists of five LPFs and each LPF is connected to an input switch driven by a 20% duty-cycle periodic clock. The switches are made with NMOS transistors, which are switching sequentially between the ON and OFF modes. The NMOS switch passes a small signal well while the PMOS switch passes a large signal well. In addition, input signal to the band-pass is much smaller than supply voltage. Therefore, the NMOS switch is chosen in this design instead of PMOS switch for maximizing input/output signal range when body effect is taken into account. Combining the NMOS and PMOS into a transmission gate (TG) can pass well both large and small signal at the price of larger layout area and need for two complementary clocks. Switch resistance can have strong impact on the maximum achievable rejection in N-path filters. In order to increase the maximum rejection of the filter, the switch resistance should be very small with respect to the source resistance. Increasing switch size will improve linearity and decrease the switch resistance. However, larger switch size also means larger parasitic capacitors, affecting the frequency range, clock leakage and also requiring more clock power to drive the switches [27]. From the other hand, the propagation delays of the NMOS switch is estimated as

$$t_{PHL-SW} = t_{PLH-SW} = 0.7R_{sw}C_{tot} \quad (3.14)$$

where  $t_{PHL-SW}$  and  $t_{PLH-SW}$  are the high-to-low and low-to-high delay of the switch, respectively,  $R_{sw}$  is the switch resistance of the NMOS switch and  $C_{tot}$  is the total capacitance on the output of the switch, that is, the sum of the output capacitance, any capacitance of interconnecting lines

and the input capacitance of the following states. Increasing switch size reduces the propagation delays from the input to the output of the switch. However, the delay in turning the switch on is increased due to higher input capacitance. Therefore, the sizes of the NMOS switches were optimized during simulation ( $W/L=3\text{ }\mu\text{m}/100\text{ nm}$ ).

### 3.3.4 Measurement Results

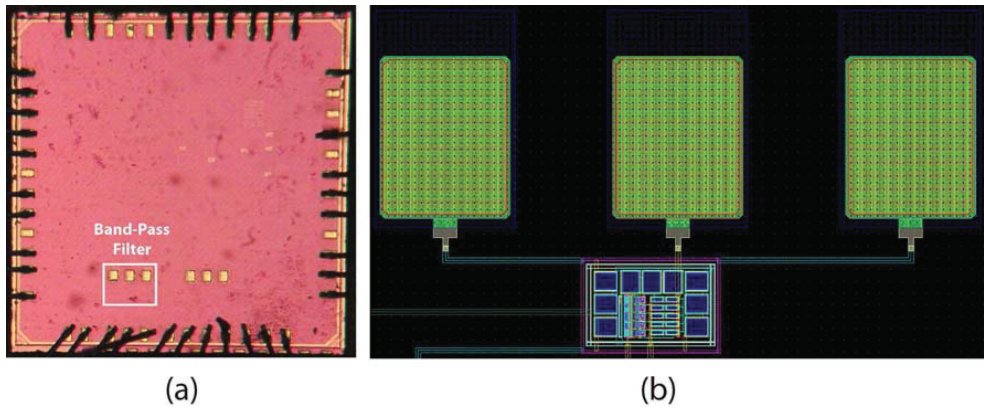
In order to verify the performance of the filter, a chip prototype was implemented in TSMC 90 nm CMOS [Paper I]. Fig. 3.5 shows the die microphotograph of the proposed filter. The filter core occupies an area of only  $0.075\times 0.055\text{ mm}^2$ . Due to the filling structures, the planarization of metal layers and the passivation layer in this 90 nm CMOS technology, the chip photo does not show any details of the circuitry. Fabricated dies were bonded directly to FR4 PCBs to avoid the inductive load of a package and to avoid long bond wires. The input of the filter was matched to  $50\text{ }\Omega$  for measurement purpose. Input RF interface was connected to a SMA connector. Adopted  $50\text{ }\Omega$  transmission line, the RF signal path was carefully designed and isolated. The output of the filter was measured by means of on-chip probing. The probe pads were designed for ground-signal-ground (GSG) probes with  $100\text{ }\mu\text{m}$  pitch. A Rohde & Schwarz ZVB20 vector network analyzer was used for measuring S-parameters as well as phase responses. The measurement setup for the filter is shown in Fig. 3.6.

In this technology, operation center frequency up to 4.4 GHz can be expected. The filter responses at different switching frequencies are plotted in Fig. 3.7. Tuning the back-gate bias voltage of the PMOS devices in the ring oscillator results in a frequency tuning range of 9.5% around 4.2 GHz. Fig. 3.8 demonstrates the phase behaviour of the filter. As can be seen, the filter expresses a linear phase shift over the designed band between 3 GHz and 5 GHz. The phase linearity ensures minimal dispersive distortion of UWB pulses. The distortion is then verified again by applying a fifth derivative Gaussian pulse at the input of the filter and then looking at the output signal on an oscilloscope. The pulse fills a bandwidth from 3.1 GHz to 5.4 GHz and as expected, no dispersion is added by the filter when the main part of the output pulse is well preserved. Both input and output signal are plotted in Fig. 3.9 indicating some attenuation of the filtered signal. The noise performance was measured by gain method using a Rohde & Schwarz FSQ26 signal analyzer. It reveals that the NF is approximately 14 dB. This high NF is due to the high filter's insertion loss (12 dB) as a result of input mismatching. The wideband filter consumes a power of 1.1 mW from a 1.2 V supply voltage.

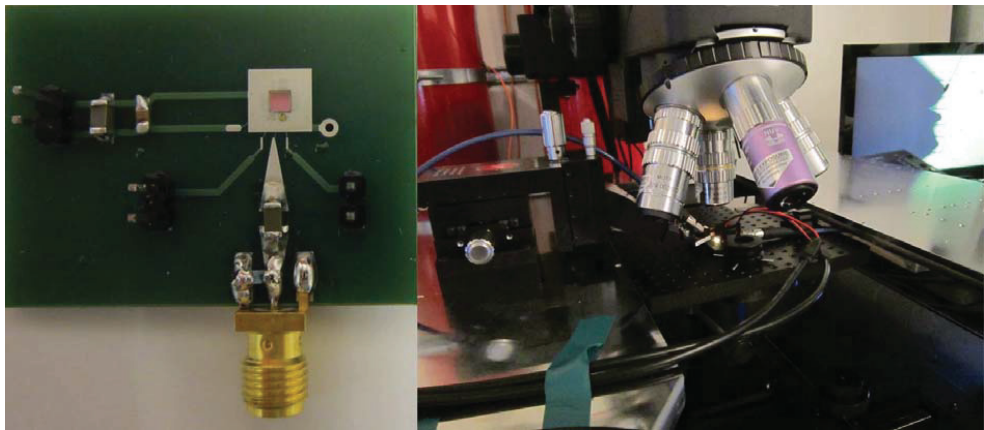
## 3.4 Proposed UWB SC 6-Path Band-Pass Filter

### 3.4.1 6-Phase Clock Generator

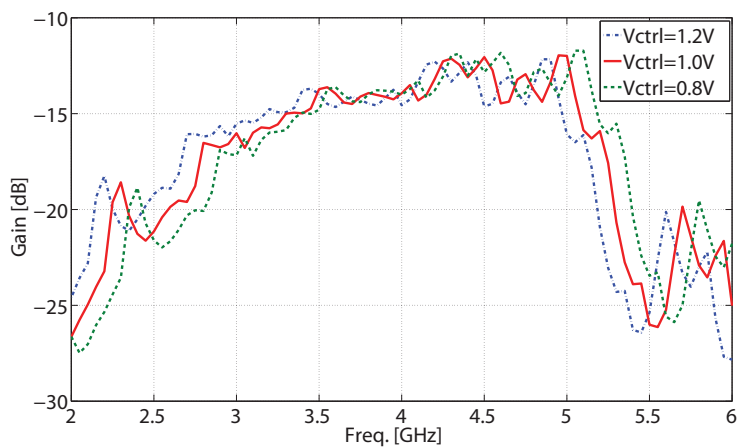
In this section, a novel ring oscillator based 6-phase clock generator is proposed. A minimum three-stage ring oscillator provides oscillation resulting in a very high-frequency clock suitable



**Figure 3.5:** The die microphotograph (a) and the layout (b) of the proposed BPF.



**Figure 3.6:** The measurement setup for the filter.



**Figure 3.7:** The measured filter responses at different center frequencies.

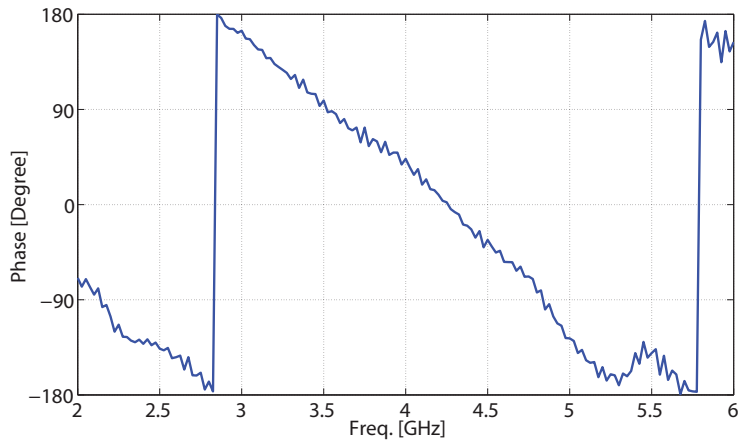


Figure 3.8: The measured phase response.

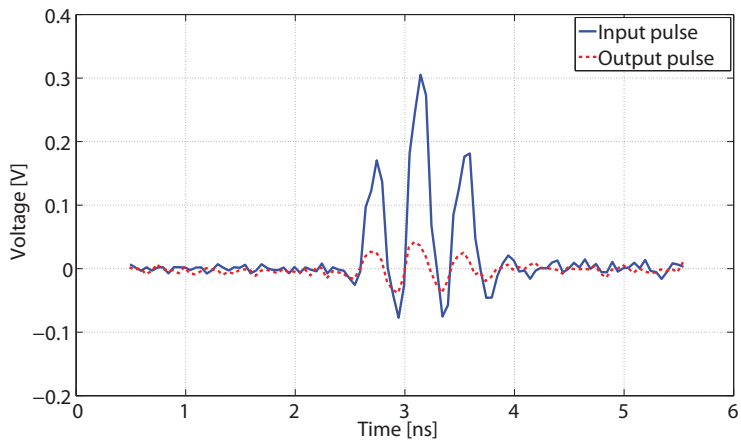
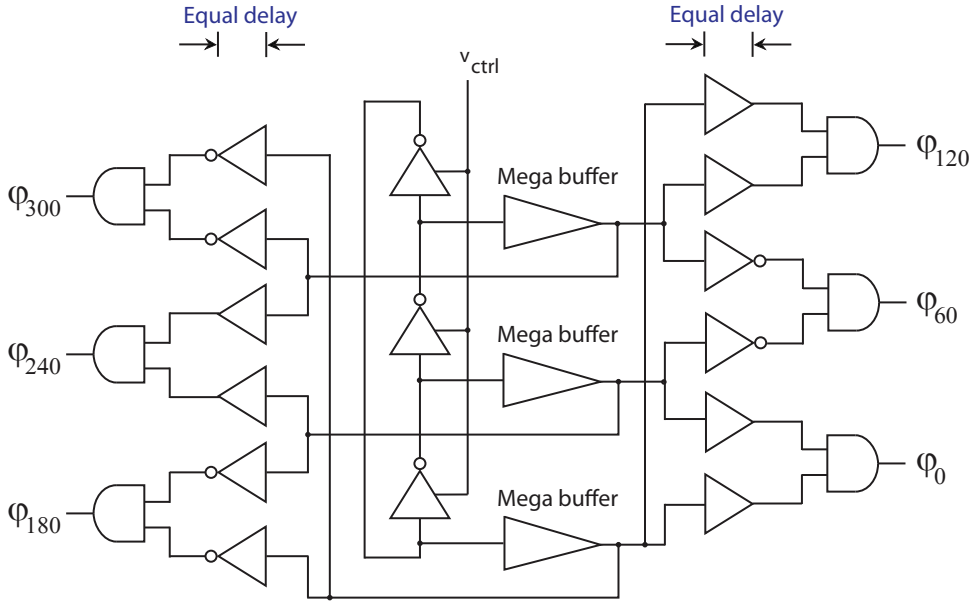


Figure 3.9: The measured input/output of fifth derivative Gaussian pulse.





**Figure 3.10:** The proposed 6-phase clock generator.

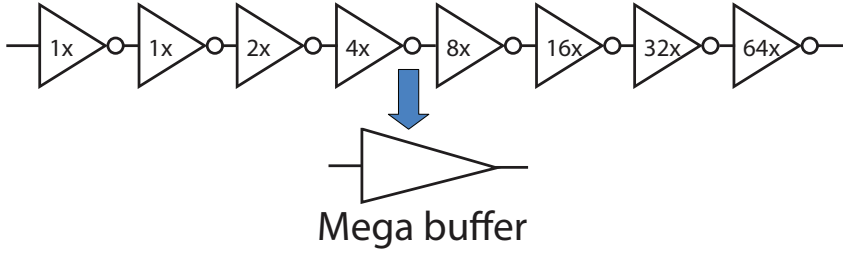
for UWB applications. The oscillation frequency,  $w_0$  is given by

$$f_0 = \frac{1}{3(t_{\text{PHL-INV}} + t_{\text{PLH-INV}})} \quad (3.15)$$

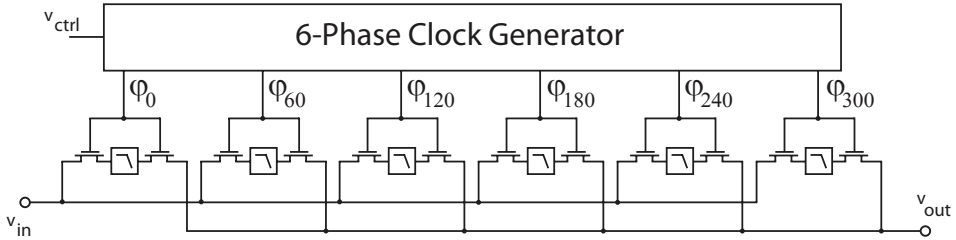
Fundamentally, the number of inverters in the ring oscillator equals to the number of clock phases needed. However, both rising and falling edges present in the ring oscillator can be exploited for twice as many clock phases. The 6-phase clock generator is shown in Fig. 3.10. Since the frequency of oscillation depends on the inherent inverter delay plus whatever additional loading is applied, taps from the delay line must have minimal load for maximum operation frequency. Consequently, a buffer with very low input capacitance is required to minimize the load capacitance while having the capability of driving large loads at the output. Fig. 3.11 shows a buffer with incremental loading for optimal performance. The oscillation frequency can be tuned by varying the time delay of each inverter stage in the ring through the bulk voltage of the PMOS transistor. In this way no additional loading is applied, thus maintaining the highest possible oscillator frequency.

### 3.4.2 Post-Layout Simulation Results

In order to ensure proper operation, post-layout simulation results of the tunable SC N-path BPF, depicted in Fig. 3.12, are provided [Paper V]. Simulated results of the filter for TSMC 90 nm CMOS were achieved using the Cadence design environment. The multiphase clock generator generates a 6-phase clock used for driving SC circuits. The bandwidth of the BPF



**Figure 3.11:** The buffer with suitable fan-out.



**Figure 3.12:** The proposed UWB SC 6-path BPF.

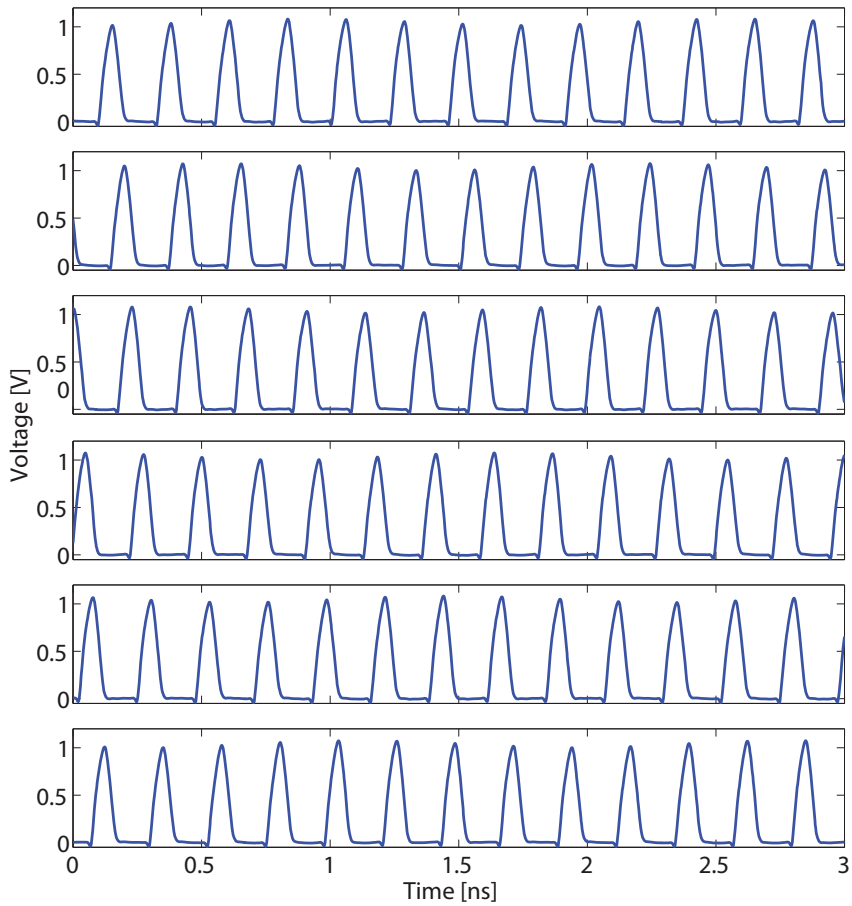
is shaped by the duty cycle of the clock and the LPF cut-off frequency. Fig. 3.13 shows an example of a 6-phase clock generated by the proposed multiphase clock generator including extracted parasitic components. In this technology, operation center frequency up to 7 GHz can be expected. However, the mega buffer can only work well up to 4.5 GHz.

Tuning the back-gate bias voltage of the PMOS devices in the ring oscillator results in a frequency tuning range of 9.3% around 4.3 GHz. The filter responses at different center frequencies are shown in Fig. 3.14. Post-layout simulation shows a noise figure from 7 dB to 8 dB as presented in Fig. 3.15.

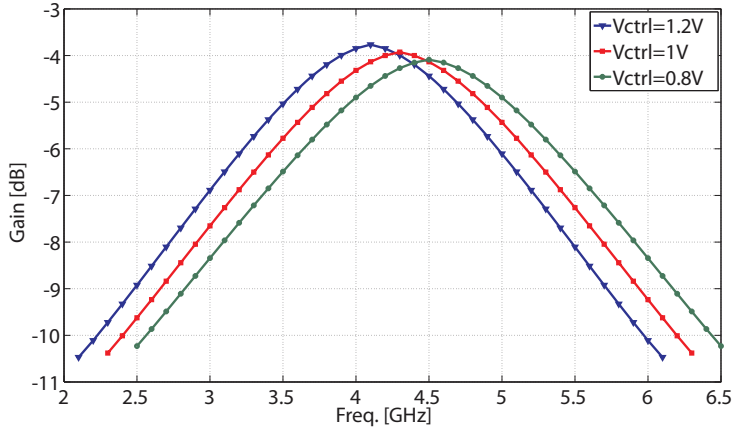
The UWB filter consumes a power of 4.5 mW from a 1.2 V supply voltage. The layout is

**Table 3.1:** Comparison with previous published tunable BPFs

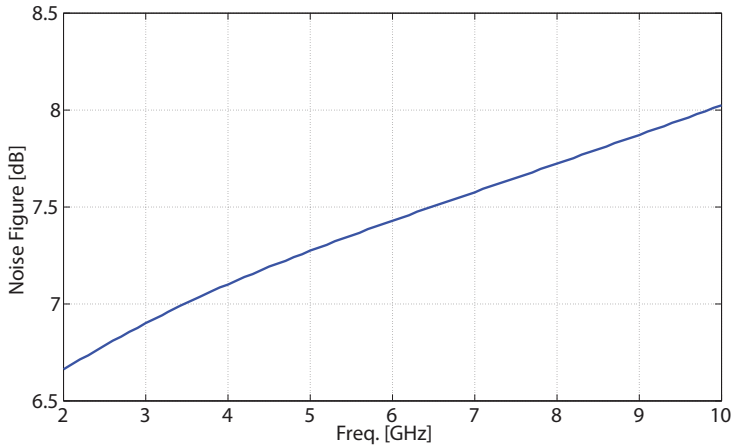
Ref.	CMOS tech.	Die area mm <sup>2</sup>	Power cons. (mW)	Voltage gain (dB)	-3 dB bandwidth (MHz)	Freq. tuning range (GHz)	NF (dB)
[24]	0.35 $\mu$ m	1.9	63	-2	1.75–4.6	0.24–0.53	9
[27]	65 nm	0.07	2-16	-2	35	0.1–1	3–5
[34]	0.18 $\mu$ m	0.81	17	0	130	2–2.06	15
[35]	0.35 $\mu$ m	0.1	5	-5	53.8	1.93–2.19	26.8
[36]	0.5 $\mu$ m	0.15	43.2	-15	80	1.77–1.86	28
[37]	0.5 $\mu$ m	2.5	15	23	70	2.45–2.85	6
This work 1	90 nm	0.004	1.1	-12	2000	4–4.4	14
This work 2	90 nm	0.007	4.5	-4	2500	4.1–4.5	7–8



**Figure 3.13:** An example of a 6-phase clock generated by the proposed multiphase clock generator.

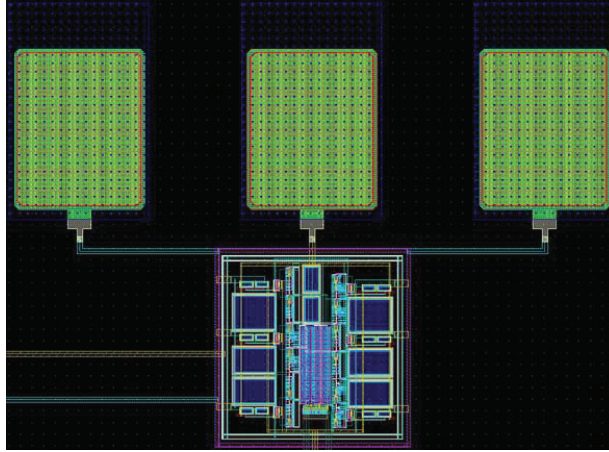


**Figure 3.14:** The simulated filter response at different center frequencies.



**Figure 3.15:** The simulated noise figure of the BPF.

shown in Fig. 3.16. The filter core occupies an area of  $0.085 \times 0.085 \text{ mm}^2$  including on-chip decoupling capacitors. Table 3.1 summarizes the performance of the filter and compares it to other published designs. Ahmed et al. [24] proposed a 8-path high-Q BPF utilized in SAW-less receiver. However, this filter consumes much power as well as large die area. In [27], a differential 4-path filter combined with a broadband off-chip transformer was realized in 65 nm CMOS. The differential architecture can reduce clock-leakage and suppress selectivity around even harmonics of the clock. Q-enhanced techniques [34]- [37] can improve filter quality factor but degrade linearity and noise. Our proposed filter offers the smallest area and highest center frequency of all the filters reported in table 3.1.



**Figure 3.16:** The filter layout:  $0.085 \times 0.085 \text{ mm}^2$ .

### 3.5 Conclusion

In this chapter, we have presented inductorless SC 5-path/6-path band-pass filters based on N-path periodically time-variant networks implemented in standard CMOS technology [Paper I][Paper V]. The proposed filters are targeted for low band of the UWB spectrum from 3 GHz to 5 GHz. As a part of the filter, novel multiphase clock generators are proposed suitable for RF frequencies. The multiphase clock generators are built with digital logic gates, thus can be easily scaled to finer pitch technology. The filter is compact, suitable for standard digital technology and can be fully integrated without any external clock reference. This filter is competitive to other start-of-the-art tunable BPFs and could substitute passive SAW filters for broadband wireless radio-communication.



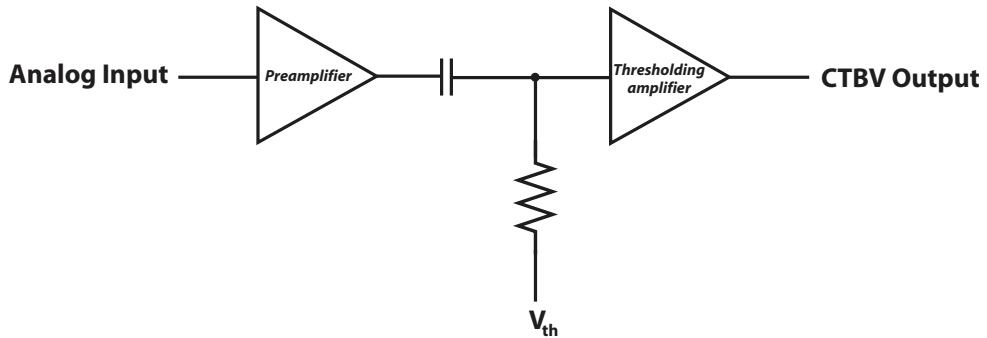
# Chapter 4

## UWB QUANTIZERS

### 4.1 Introduction

At the Nanoelectronics group, Department of Informatics, University of Oslo, we have brought forward the Continuous-Time Binary-Value (CTBV) design paradigm [5] acknowledging the strong power-limitation imposed ( $-41.3$  dBm/MHz). The CTBV approach is simply based on inherent CMOS process-dependent gate delays combined with a coarse quantizer. With a SNR often less than one, using a single-bit (binary) quantization may be sufficient. These systems do need significant processing gain (integration) for proper operation. CTBV impulse radar solutions are now commercially available [38] and high-precision ranging receivers have been demonstrated [39]. An essential building block of the CTBV system is a wideband single-bit quantizer or thresholder continuously comparing the incoming signal to a threshold voltage, giving a binary or digital output of the sign of the comparison which is CTBV coded signal. In fact, sweeping the threshold quantization voltage enable quantization of any incoming signal. Such a function can be obtained with a high-gain comparator. In [40], a 4 GS/s 4-bit flash ADC in  $0.18\text{ }\mu\text{m}$  CMOS was presented and comparators with four stages and integrated inductors were implemented. Such inductors usually need a large chip area. In [41], a comparator was designed for an analog rank-order extractor and in [42], a latch-type voltage sense amplifier for a SRAM is described. Conventional comparators are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback combined with a clocked reset [40] - [45], but such an approach cannot be used for continuous time systems. By avoiding a high frequency sampling clock, power-efficient solutions exist even for CTBV systems.

The basic principle on which quantizer is based is shown in Fig. 4.1. The previous stages such as LNA constitute a preamplifier. The preamplifier amplifies the input signal by a small amount before it is coupled through a capacitor with a DC-setting resistor on the other side. The DC value of this node will be  $V_t$  and the amplified input signal will then swing around this voltage. Whenever the voltage of this node is above the operating point of the thresholding amplifier, its output will be "1" and otherwise, it will be "0". A second effect of the coupling capacitor and the DC-setting resistor is that they will act as a high-pass filter for the input signal, thus rejecting low-frequency signals which could otherwise cause masking problems. By using an equivalent resistance circuit with a tunable value instead of a resistor, for example, a



**Figure 4.1:** Quantizer with a tunable threshold level.

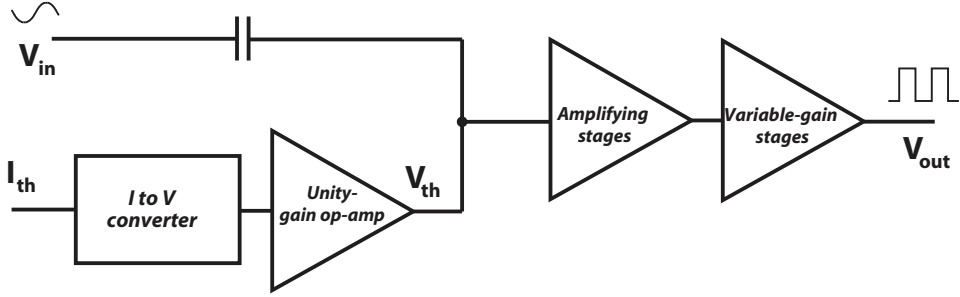
transconductance amplifier, it is possible to make the cut-off frequency of the high-pass filter tunable. It is shown in [5] that the higher the preamplifier gain is, the lower the flicker noise introduced by the thresholding amplifier will be compared to the input signal. So by amplifying the input signal as much as possible without causing any other problems, the flicker noise will be reduced by a factor corresponding to the gain of the preamplifier. The AC coupling before the thresholding amplifier will filter out any flicker noise created by the preamplifier. However, if the input signal is amplified too much, the tuning range of  $V_t$  will not be able to cover the full extent of the input signal, thus the circuit will not perform as expected.

In this chapter, several solutions for a continuous-time UWB quantizer with tunable threshold setting targeted for IR-UWB receiver front-ends are proposed [Paper III][Paper IV][Paper VII][Paper IX]. For quantization performance, linearity is insignificant. Therefore, in the design of all quantizers, gain and noise performance are optimized trading off linearity. Area savings from reduced linearization circuitry also drives down production cost and offer greater commercialization advantages.

## 4.2 Proposed UWB Variable-Gain Single-Ended Quantizer

This section presents a novel variable-gain single-bit UWB quantizer suitable for baseband receiver front-end fabricated in 90 nm CMOS technology. By avoiding high frequency sampling clock, power consumption is only 4.8 mW making the proposed quantizer suitable for low-power wireless communications. The prototype chip is tested and measurement results are provided. The quantizer topology is proposed in Fig. 4.2. It consists of a threshold circuit, cascaded amplifier stages with fixed gains in combination with variable gain stages. The input signal is added with the threshold voltage providing controllable quantization voltage levels for input signal thresholding. Therefore, the DC needs to go through amplifying stages preventing from using of any architecture that is AC-coupled.





**Figure 4.2:** The architecture of the proposed variable-gain single-bit UWB quantizer.

### 4.2.1 Amplifying Stages

A quantizer with programmable gain may be preferred in order to control the RF power to an optimum level since received signals can have a large range of amplitude variations depending on the instantaneous signal strength. A simple digital inverter with resistive feedback is used as wideband amplifier. The inverter structure is chosen in this design since its output voltage swings from VDD to ground unlike other amplifiers that never quite reach the supply level. In addition, the static power dissipation of the CMOS inverter is practically zero. Without employing resistive feedback, amplifier bandwidth is mainly determined by RC time constants of every node. In CMOS technology, severe parasitic capacitance deteriorates bandwidth significantly. The adding of feedback resistance increases the output pole to higher frequency hence extends the bandwidth. However, there is a trade-off between the gain and the bandwidth of the amplifier. For increased bandwidth, stage gain is sacrificed for strong feedback. Wider bandwidth is obtained at the expense of lower gain per stage by using low values of feedback resistance  $R_f$ . In order to recover gain, a cascade of twelve inverters is used as demonstrated in Fig. 4.3. From another point of view, to reduce jitter, the ratio of the PMOS width to the NMOS width,  $W_p/W_n$  that brings the inverter switching point close to  $V_{DD}/2$  should be chosen. However, a very large value leads to a large input capacitance and hinders high-speed operation. Shortest propagation delay is expected to result from  $1.5 < W_p/W_n < 2$  [46]. In this design,  $R_f \approx 7.8 \text{ k}\Omega$  and  $W_p/W_n = 3$  were optimized in favour of wide bandwidth and low jitter, respectively.

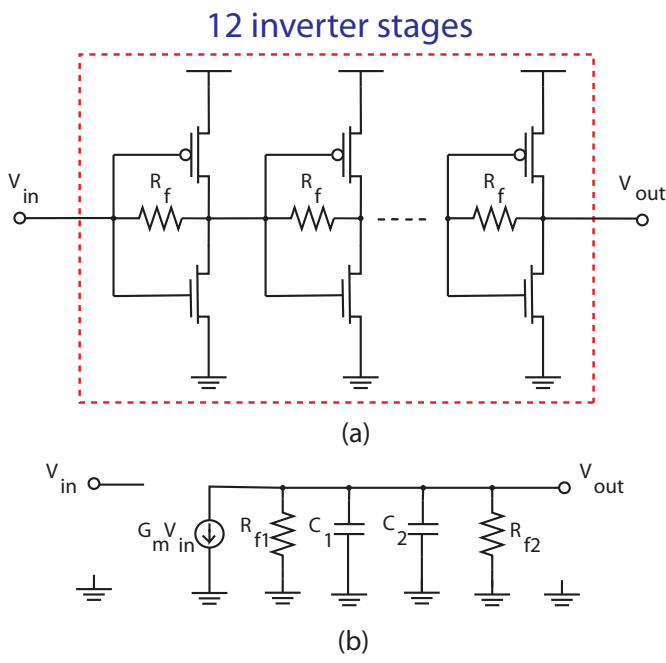
Considering the inter-stage small-signal model, the transfer function can be expressed as [47]

$$\frac{V_{out}}{V_{in}} = \frac{-G_m R_T}{1 + s C_T R_T} \quad (4.1)$$

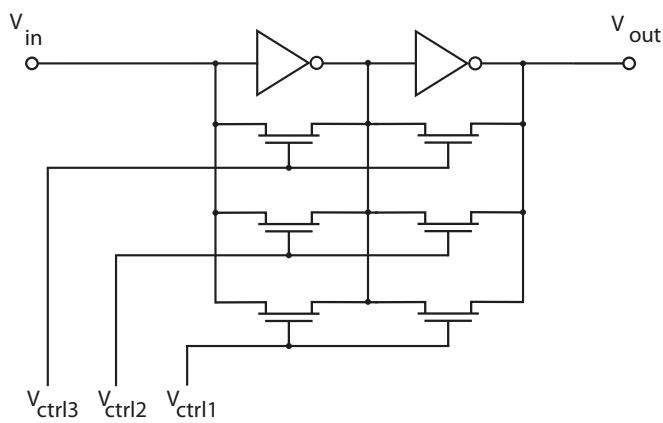
where  $R_T$  denotes  $R_{f1} || R_{f2} \approx 3.9 \text{ k}\Omega$  and  $C_T$  represent  $C_1 + C_2$ .  $R_{f1}/R_{f2}$  and  $C_1/C_2$  denote equivalent resistors and capacitors contributed by previous and next stages, respectively.

### 4.2.2 Variable Gain Stages

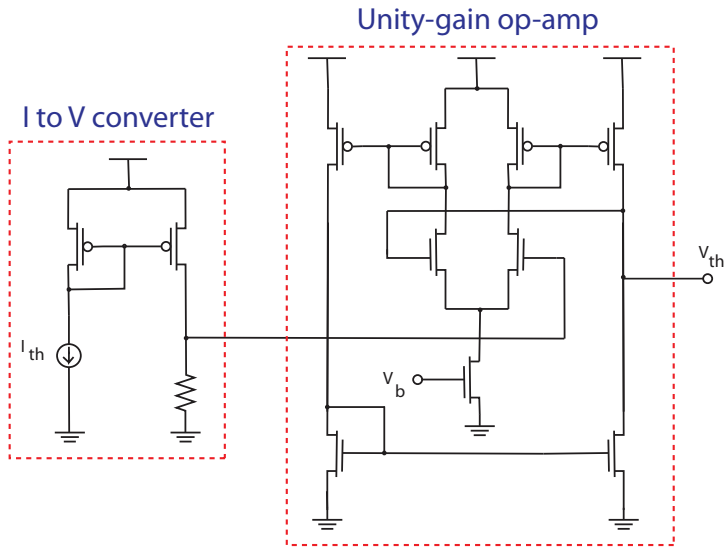
Several circuit topologies for variable gain amplifiers have been proposed in the literature. Most conventional CMOS variable gain amplifiers employ multistage architecture and combine several



**Figure 4.3:** (a) Resistive-feedback inverter stages. (b) Equivalent inter-stage small-signal model.



**Figure 4.4:** The variable gain stages.



**Figure 4.5:** The threshold circuit of the quantizer.

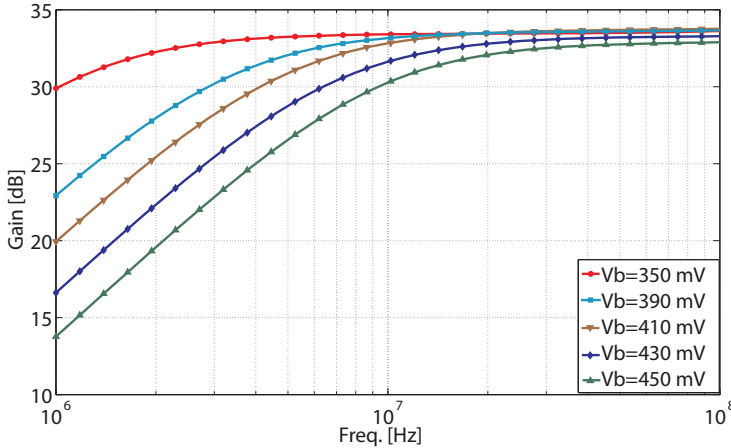
gain stages with a gain control circuit to satisfy the specifications of radio communications. Generally, variable gain is realized by changing the gain transfer function of an amplifier according to a gain control signal. This can be obtained by current steering, controlling the feedback or bias current. A convenient way to add programmable gain is to control the feedback loop as exploited in Fig. 4.4. Binary control signals are provided by switching on one or more of these feedback connections. Again, we are exploring the simple inverter for large bandwidth combined with suitable different sized feedback transistors.

### 4.2.3 Threshold Circuit

The threshold circuit is depicted in Fig. 4.5. In order to reduce noise, a threshold current,  $I_{th}$  is used as input.  $I_{th}$  is then converted into a suitable threshold voltage,  $V_{th}$  by a simple I-V converter followed by a unity-gain op-amp. The I-V converter acts as a linear circuit with transfer ratio  $k = V_{th}/I_{th}$ . By changing  $V_b$ , the tail current of the unity-gain op-amp, driving strength can be changed in the mixing node as well as changing the corner frequency of the first-order high-pass filter constituted by the input coupling capacitor and the equivalent transconductance of the threshold driving circuit. Fig. 4.6 shows the post-layout simulation of the low-frequency gain response corresponding to different  $V_b$  settings. When  $V_b$  is set between 350 mV and 450 mV, the -3 dB bandwidth toward the lower end of the frequency band can be tuned to 10 MHz.

### 4.2.4 Measurement Results

The quantizer was fabricated in TSMC 90 nm [Paper IV] CMOS. Circuit design at high frequencies involves more detailed design than at lower frequencies when the effect of parasitic

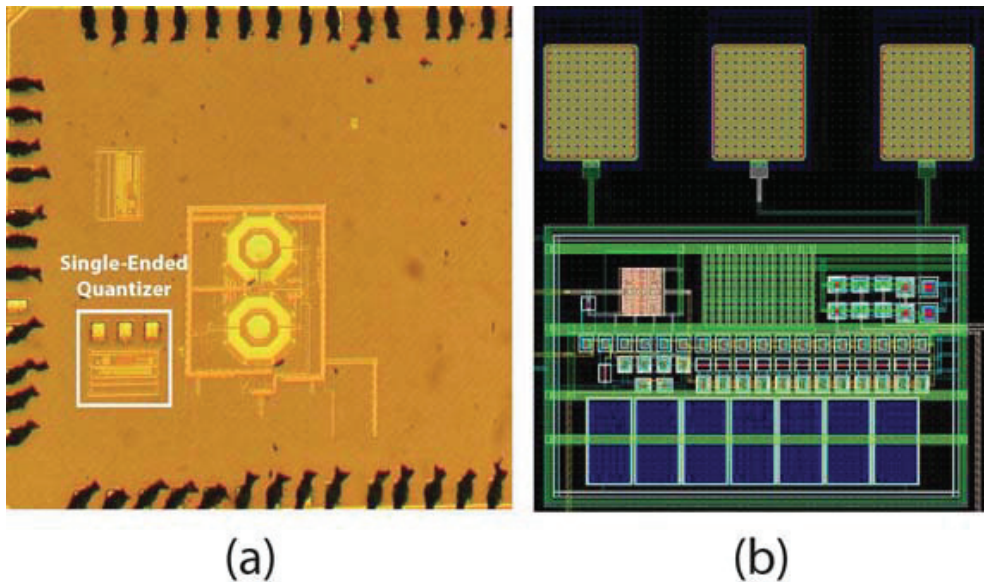


**Figure 4.6:** The simulated low-frequency gain response at different  $V_b$  settings.

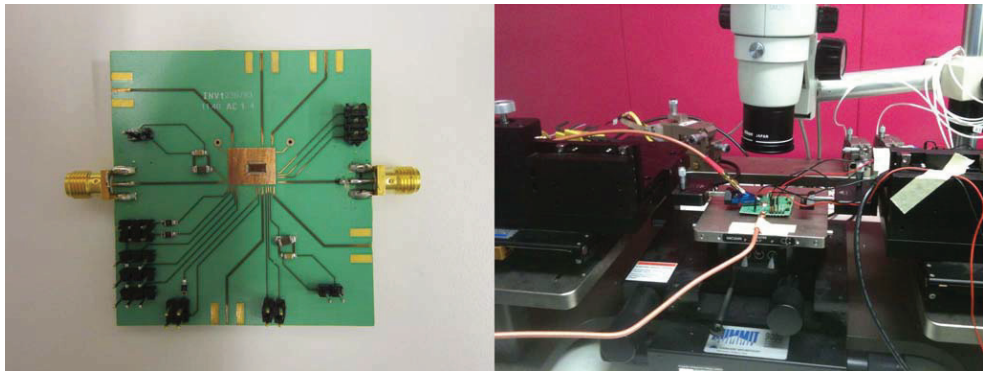
capacitances and inductances can impose serious constraints on performance. Thus, all components excluding decoupling capacitors are RF models provided by TSMC. A Rohde & Schwarz ZVB20 vector network analyzer has been used for S-parameters measurement of the quantizer while the NF was measured by gain method using a Rohde & Schwarz FSQ26 signal analyzer. Fig. 4.7 shows the die microphotograph of the proposed quantizer. By avoiding the use of broadbanding techniques such as peaking inductors as exploited in [47] [48], the proposed quantizer only occupies a die area of  $0.25 \times 0.17 \text{ mm}^2$ . For measurement, fabricated dies were bonded directly to Rogers PCBs to avoid the inductive load of the package and to avoid long bond wires. The measurement setup for the quantizer is shown in Fig. 4.8.

The input of the quantizer is matched to  $50 \Omega$  for measurement purpose. Input RF interface was connected to a SMA connector. Adopted  $50 \Omega$  transmission line, the RF signal path was carefully designed and isolated. The transmission line is located as close as possible to the high frequency input pad to reduce the length of bond wire as well as the parasitic series inductance. The input is DC isolated using an on-chip capacitor. The output of the quantizer was measured by means of on-chip probing. The probe pads were designed for ground-signal-ground (GSG) probes with  $100 \mu\text{m}$  pitch. The measured input return loss is plotted in Fig. 4.9. For most desired frequencies, the input return loss is less than  $-10 \text{ dB}$  indicating that the reflection coefficient is less than  $0.3$  over the bandwidth from  $10 \text{ MHz}$  to  $2.7 \text{ GHz}$ .

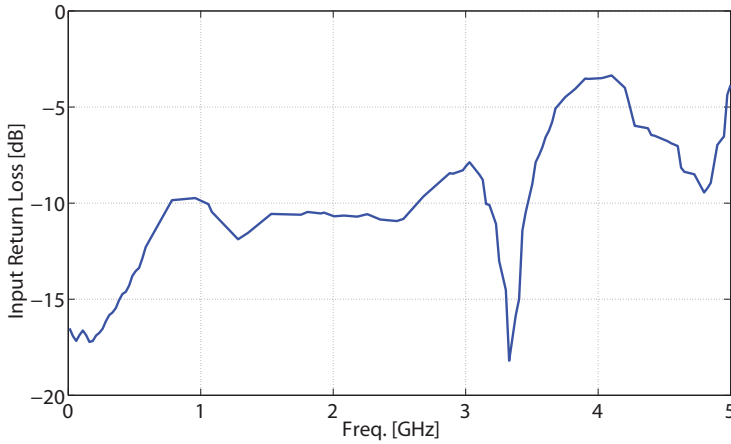
Fig. 4.10 illustrates the measured and simulated gain of the quantizer in the highest gain mode. The measured results are in good agreement with the simulated ones. A high gain of approximately  $33 \text{ dB}$  over the  $-3 \text{ dB}$  bandwidth of  $10 \text{ MHz}$ – $2.7 \text{ GHz}$ , is demonstrated. Furthermore, by tuning on/off the MOSFETs in the feedback loop, a gain tuning range of  $10 \text{ dB}$  is obtained with insignificant increase of the noise figure. At frequencies beyond  $2.7 \text{ GHz}$ , the measured gain response differs from the simulated one. This is probably due to bond wire inductances combined with parasitic capacitances limiting the bandwidth as well as changing the high-frequency impedance matching. The quantizer's bandwidth can be extended to FCC band by applying suitable bandwidth enhancement techniques. These techniques utilize inductors trading off bandwidth versus large chip area and power consumption. The phase response of the



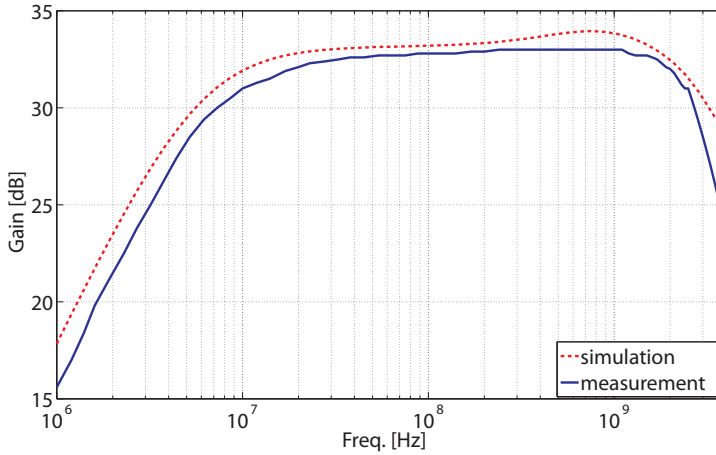
**Figure 4.7:** The die microphotograph (a) and the layout (b) of the proposed single-ended quantizer.



**Figure 4.8:** The measurement setup for single-ended quantizer.



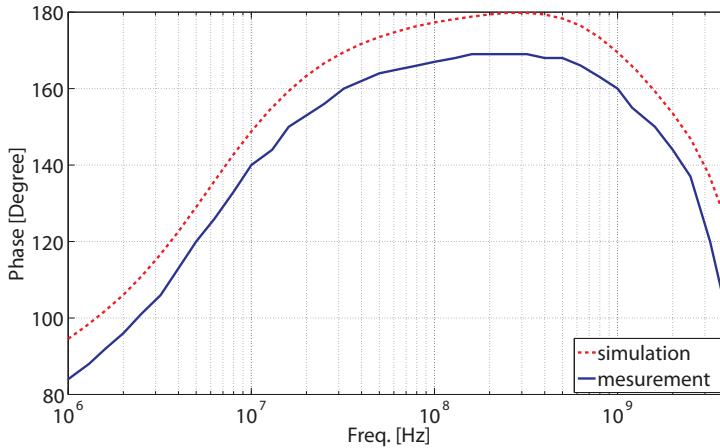
**Figure 4.9:** The measured input return loss of the quantizer.



**Figure 4.10:** The measured and simulated gain response at  $V_b = 420$  mV.

quantizer is plotted in Fig. 4.11. The gain-crossover frequency of the quantizer is 6.2 GHz while the phase at that frequency is around  $80^\circ$ . This leads to a phase margin of approximately  $260^\circ$ , thus the quantizer should be unconditionally stable.

The noise performance is also measured at various gain settings. It reveals that the NF is between 7 dB and 10 dB. Fig. 4.12 demonstrates the measured performances of the quantizer when a 2 GHz and sinusoidal signals are applied at the input for some threshold levels. The threshold level is tuned by programming a microcontroller connected to a digital-to-analog converter (DAC). Therefore, the quantizer threshold can be varied by varying the DAC values. Even for small input signal, a binary value should appear at the output. The input signal can have a minimum amplitude of 45 mV peak to peak. The output is seen by an Agilent Infiniium 54855A oscilloscope. When the threshold current,  $I_{th}$  is equal or greater than  $95.87 \mu\text{A}$ , the threshold is set below the input signal. As a result, the output of the quantizer is always at high level.

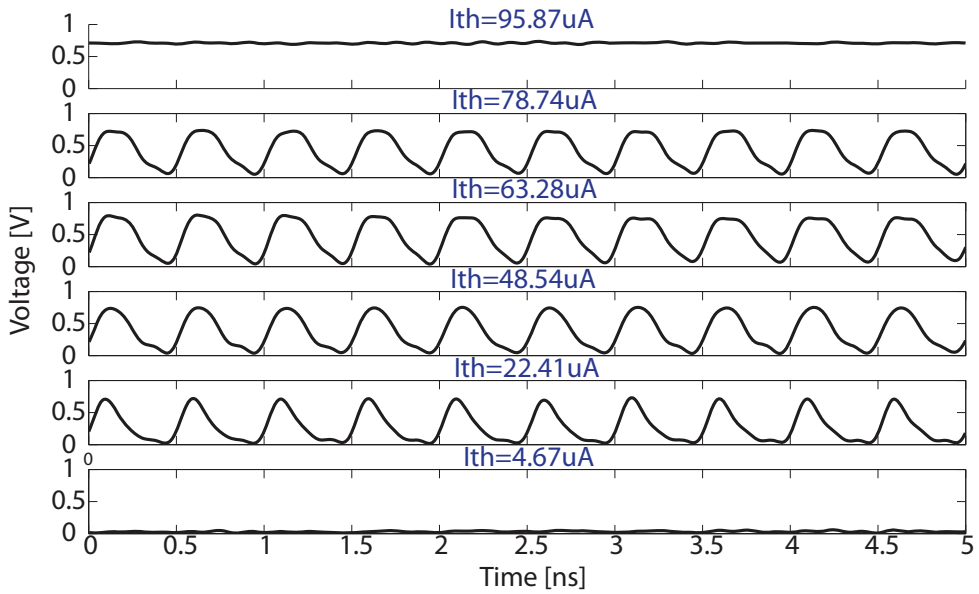


**Figure 4.11:** The measured and simulated phase response at  $V_b = 420$  mV.

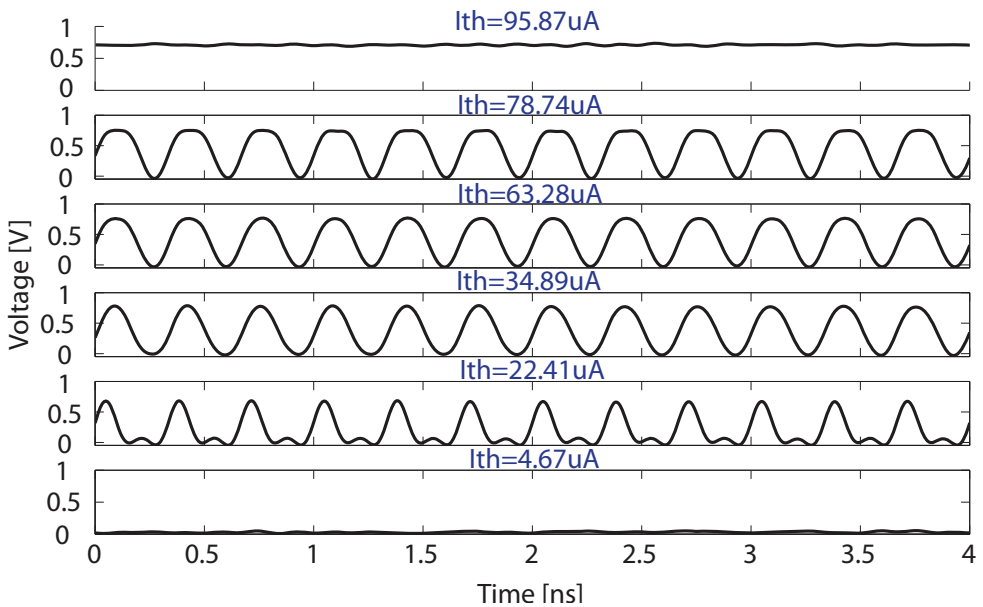
**Table 4.1:** Comparison with the previous published variable gain amplifiers

Ref.	CMOS tech.	Die area (mm <sup>2</sup> )	Power cons. (mW)	Gain (dB)	-3 dB BW (GHz)	NF (dB)
[49]	90 nm	0.01	2.5	-10–50	2.2	17–30
[50]	0.18 $\mu$ m	0.7	40	-16–34	2	N/A
[51]	0.18 $\mu$ m	0.42	20.5	-39–55	0.9	6.8
[52]	0.18 $\mu$ m	0.7	41.4	10–22	0.8	4.2–6
[53]	90 nm	0.36	32.5	0–45	0.5	16
This work	90 nm	0.04	4.8	23–33	2.7	7–10

Conversely, when  $I_{th}$  is equal or smaller than  $4.67 \mu\text{A}$  corresponding to the threshold is above the input signal, the output is always at low level. When the threshold current is somewhere between those two values, the input signal is quantized as can be seen in the figure. For a 45 mV peak-to-peak input signal, measurement results reveal that the range of the threshold current is approximately  $90 \mu\text{A}$ . As required, even minor signal perturbations are quantized. At 3 GHz, the minimum input signal that the quantizer can detect is 110 mV peak to peak as illustrated in Fig. 4.13. The quantizer draws a current of approximately 4 mA from a 1.2 V supply voltage. Table 4.1 summarizes the performance of the quantizer and compares it to other published designs in silicon. The VGA in [49] was implemented using four-stage modified Cherry-Hopper amplifier. The dual feedback DC-offset cancelling network not only corrects DC offset but also extends the bandwidth. However, this yields a high noise figure. The cascaded VGA in [51] utilizes an exponential gain control function based on bipolar transistors and a control signal converter. As a result, the gain can vary for a very wide range of 94 dB. In [52] the gain tunability is obtained by means of current steering and negative gm-cell tuning. The VGA in [53] integrated with a received signal strength indicator function achieves a wide tuning range as well as high linearity trading off noise figure.



**Figure 4.12:** The measured performance of the quantizer with a 2 GHz-sinusoidal input signal.



**Figure 4.13:** The measured performance of the quantizer with a 3 GHz-sinusoidal input signal.



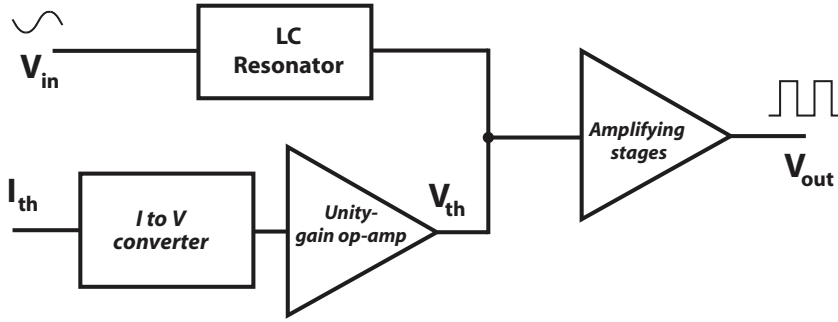


Figure 4.14: The structure of the proposed quantizer.

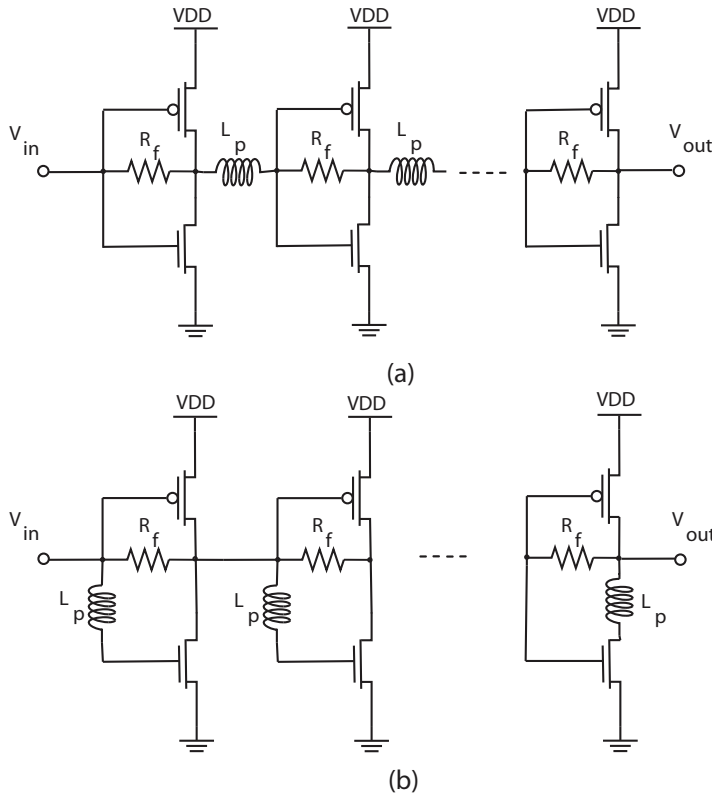
### 4.2.5 Summary

An inductorless variable-gain UWB single-bit quantizer targeted for IR-UWB baseband receiver front-end has been presented [Paper IV]. The measurements demonstrate the validity of the proposed design approach. The quantizer achieves a flat gain over the -3 dB bandwidth of 2.7 GHz. Measurement results show a gain variation range of 10 dB with a maximum gain of 33 dB while the NF is from 7 dB to 10 dB. The sensitivity is 45 mV at 2 GHz and 110 mV at 3 GHz. The sensitivity here is defined as the weakest pulse signal level that can be detected by the quantizer. The quantizer occupies a die area of  $0.25 \times 0.17 \text{ mm}^2$ . It is compact and can be fully integrated without any external clock reference.

## 4.3 Proposed 3.1–10.6 GHz Single-Ended Quantizer

In this section, a novel continuous-time CMOS quantizer whose -3 dB bandwidth covering the entire FCC UWB spectrum from 3.1 GHz to 10.6 GHz is presented. The quantizer is an area-efficient, single-inductor solution designed for TSMC 90 nm CMOS technology. The proposed quantizer circuit is shown in Fig. 4.14 [Paper IX]. It consists of cascaded amplifier stages with an input LC resonator for extended bandwidth. The threshold voltage,  $V_{th}$  is added with the input signal at the amplifier input. Again, for improved noise performance, the threshold voltage is set by a current,  $I_{th}$  and is converted to a suitable threshold voltage level matching the build-in inverter threshold.

A simple digital inverter with resistive feedback is used for each amplifier stage. However, using resistive feedback is the simplest type of broadbanding. It is also the most inefficient: lower gain, lower output power and degraded noise figure [54]. In order to extend the bandwidth, conventional multiple inductive-series peaking technique is employed in [47], which is demonstrated in Fig. 4.15a. In this architecture, inductors are deployed between each amplifier. Together with parasitic capacitances, a third-order LC-ladder filter is giving an impedance transformation network [55] [56]. Another structure with some improvement is introduced in [48] and depicted in Fig. 4.15b. By locating a peaking inductor at the gate of NMOS of each inverter stage, the -3 dB roll-off frequency can be boosted to higher frequencies. However, using peaking inductor



**Figure 4.15:** (a) Conventional multiple inductive-series peaking technique. (b) Splitting-load inductive peaking technique.

for bandwidth extension in each gain stage is area demanding.

In this design, a novel structure for the wideband amplifier is proposed. Instead of using multiple peaking inductors, a resonant peak at the amplifier corner frequency can 'pull up' the gain, thus extending the bandwidth significantly as shown in Fig. 4.16. Thus, only a single, small inductor (0.7 nH) is used for the LC resonator regardless of the number of amplifier stages. The LC resonator also acts as a high-pass filter at the input, shifting the bandwidth to higher frequencies suitable for the FCC approved UWB spectrum. Table 4.2 gives a comparison of several reported designs. The proposed amplifier architecture is shown in Fig. 4.17 [Paper VIII]. Since the LC resonator produces very low impedance at the input, a buffer is required to drive the source with negligible signal loss. A source follower configuration is proposed for this purpose. A current mirror supplies the bias current for the source-follower. Although the DC level of the output voltage is somewhat below the DC level of the input voltage, ideally the small-signal voltage gain is close to unity. By changing  $V_{bias}$  and  $I_{bias}$ , the high input impedance and moderate output impedance of the buffer can be tunable.

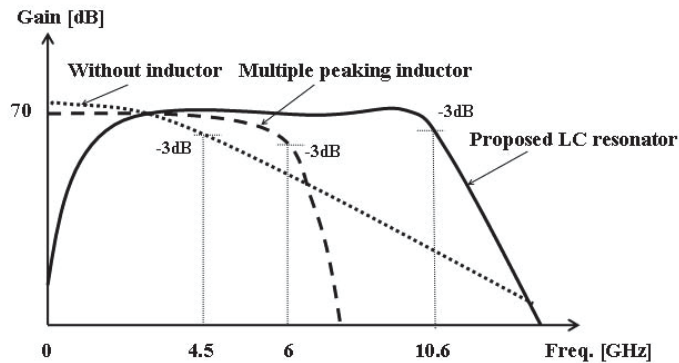


Figure 4.16: Bandwidth comparison among the designs.

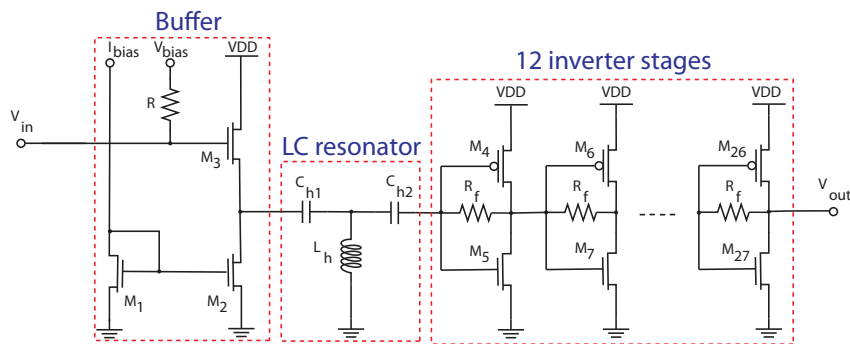


Figure 4.17: The proposed high-gain UWB amplifier.

Table 4.2: Comparison with previous published UWB amplifiers

Ref.	CMOS tech.	Die area (mm <sup>2</sup> )	Power cons. (mW)	Gain (dB)	-3 dB BW (GHz)	No. of stages	No. of inductors
[47]	0.18 $\mu$ m	0.14	70	61	DC–7.2	5	8
[48]	0.13 $\mu$ m	0.34	9.1	13.2	DC–11.5	3	3
This work	90 nm	0.12	25.1	70	3.1–10.6	12	1

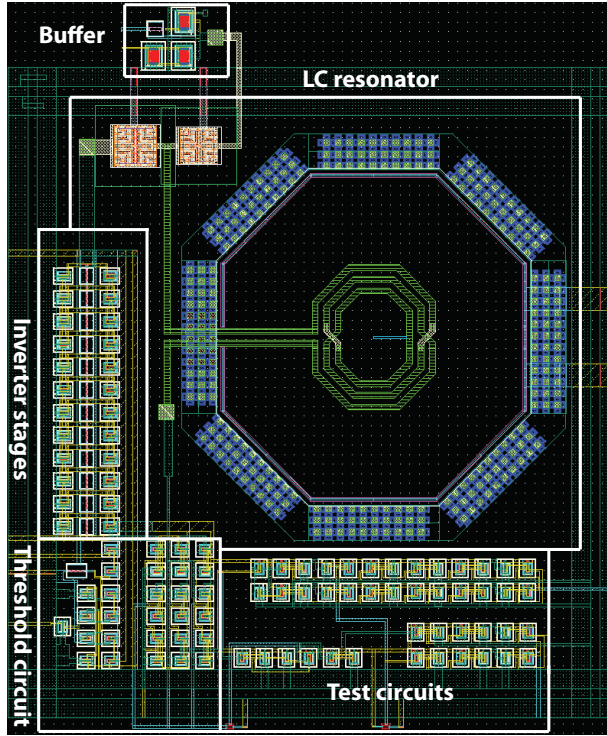


Figure 4.18: The quantizer layout:  $0.38 \times 0.32 \text{ mm}^2$ .

### 4.3.1 Post-Layout Simulation Results

Post-layout simulation results of the quantizer for TSMC 90 nm CMOS technology is achieved using the Cadence design environment. All components used for simulation are RF models provided by TSMC. The proposed quantizer occupies a die area of  $0.38 \times 0.32 \text{ mm}^2$  as shown in Fig. 4.18.

The performance of the source-follower buffer is demonstrated in Fig. 4.19. As shown in the figure, the attenuation is negligible while maintaining a flat frequency response throughout the desired frequency range between 3.1 GHz and 10.6 GHz. This ensures the efficient use of the source-follower buffer at the input. The input impedance of the amplifier is designed for matching to  $50 \Omega$ . Fig. 4.20 and Fig. 4.21 show the simulated input return loss and voltage standing wave ratio, respectively. As depicted in these figures, the amplifier presents good input matching better than -18 dB over the entire UWB spectrum while the VSWR is less than 1.6 indicating that the reflection coefficient is less than 0.2 across the desired frequency range. Fig. 4.22 plots the performance of the threshold tuning circuit. The threshold voltage changes linearly with the applied input current when varying from zero to  $100 \mu\text{A}$ . Then it becomes saturated as the current continues increasing. The range for threshold voltage,  $V_{th}$ , is between GND and 800 mV. Simulation results also show that the operating point of the quantizer is around 520 mV so the threshold level is from -520 mV to 380 mV. Fig. 4.23 shows the frequency response of the quantizer. A high gain of approximately 70 dB throughout the entire UWB spectrum,

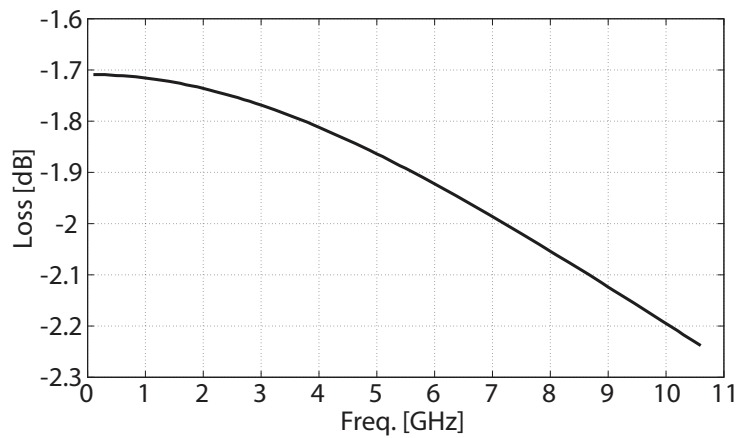


Figure 4.19: The simulated frequency response of the source-follower buffer.

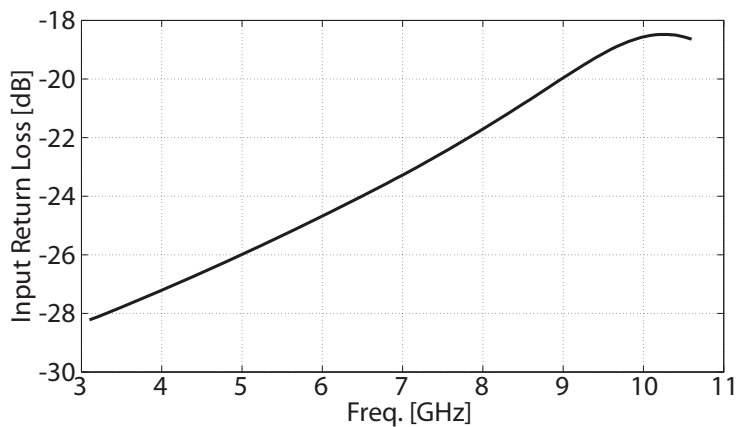


Figure 4.20: The simulated input return loss of the amplifier.

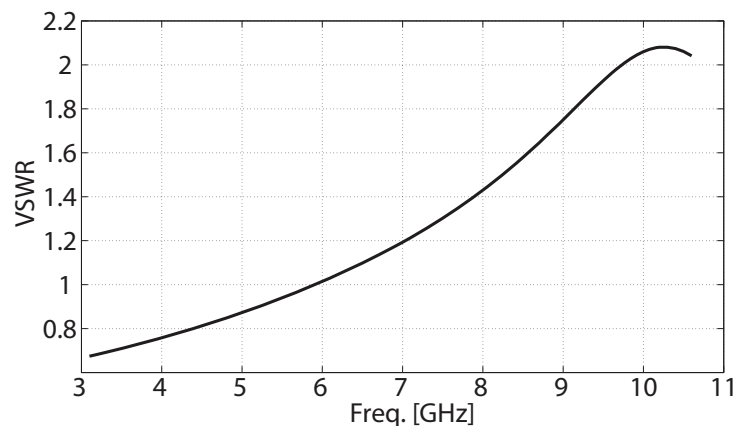
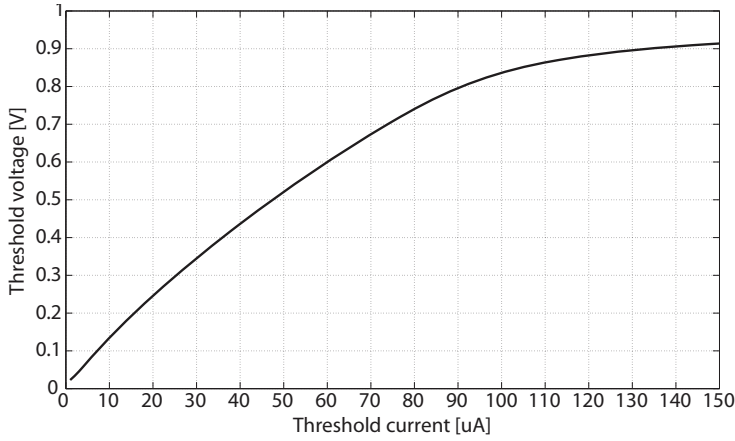
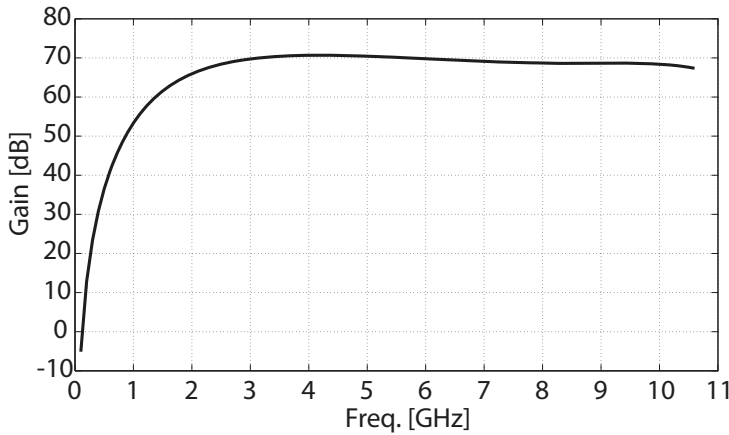


Figure 4.21: The simulated input VSWR of the amplifier.



**Figure 4.22:** The simulated performance of the threshold circuit.



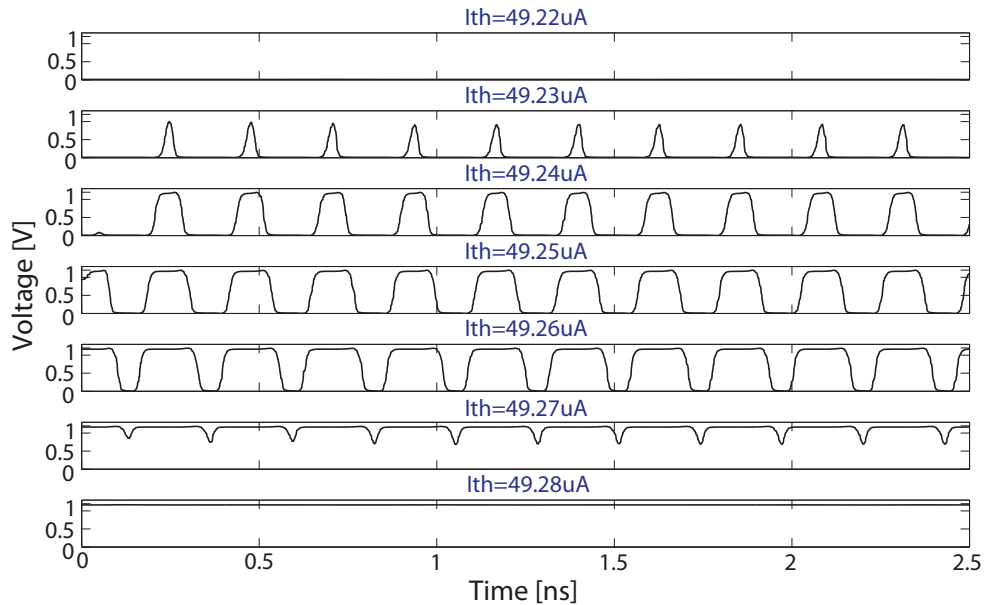
**Figure 4.23:** The simulated frequency response of the quantizer.

3.1 GHz–10.6 GHz, is demonstrated.

The Rollett's stability factor is calculated over the frequency band 3.1 GHz–10.6 GHz by equation (4.2). Since its value is always greater than unity, the circuit claims unconditional stability.

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad (4.2)$$

Fig. 4.24 gives the performance of the quantizer when a sinusoidal signal is applied at the input for some threshold levels. The input signal has the amplitude of 2.5 mV, frequency of 5 GHz. The threshold voltage is swept with the step size of 100  $\mu$ V. As required, even minor signal perturbations are quantized.



**Figure 4.24:** The simulated performance of the proposed 3.1–10.6 GHz quantizer.

### 4.3.2 Summary

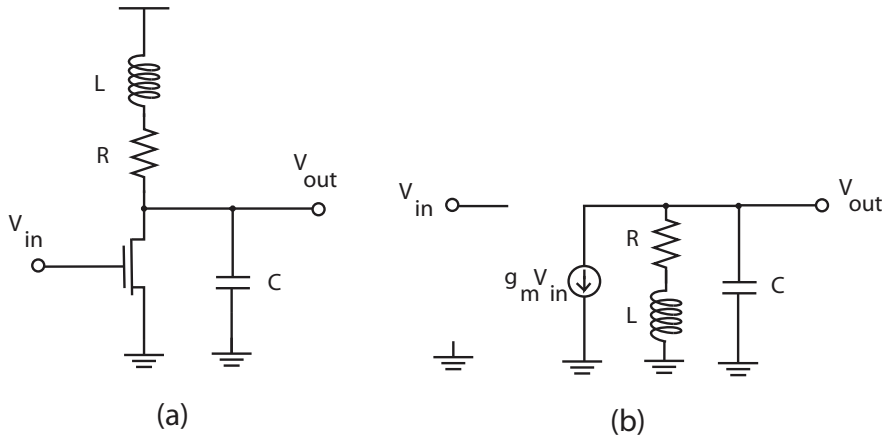
We have proposed a continuous-time, UWB quantizer with tunable threshold level and high gain suitable for FCC UWB applications [Paper IX]. The proposed quantizer achieves a -3 dB bandwidth covering the entire FCC UWB spectrum from 3.1 GHz to 10.6 GHz with a very high gain of approximately 70 dB. The quantizer is intended for CTBV architectures with low-power operation. Area-efficiency is good using only one inductor.

## 4.4 Proposed UWB Fully-Differential Quantizer

A differential approach is usually preferred to a single-ended due to improved common-mode noise performance, rejection to parasitic couplings and increased dynamic range.

### 4.4.1 Bandwidth Enhancement Techniques

Although CMOS is viable for system-on-chip solutions, its parasitics limit the performance of broadband amplifiers and motivate the use of bandwidth extension techniques. In this section, some bandwidth enhancement techniques based on inductive peaking will be introduced. Three major types of inductive peaking techniques include shunt peaking, series peaking and T-coil peaking. They use inductors to trade off bandwidth versus peaking in the magnitude response [57] [58] [Paper VII].



**Figure 4.25:** (a) A common-source amplifier with shunt peaking. (b) Equivalent small-signal model.

### Shunt peaking

Fig. 4.25 shows a common-source amplifier with shunt peaking. The gain of a purely resistively loaded common-source amplifier is proportional to  $g_m R$ . When a capacitive load is added, the gain eventually falls off as frequency increases due to the capacitor's impedance diminishes. The capacitor  $C$  is taken to represent all the loading on the output node, including the drain parasitic capacitance and the input capacitance of the next stage. The addition of an inductor in series with the load resistor provides an impedance component that increases with frequency. This also helps offset the decreasing impedance of the capacitor, leaving a net impedance that remains roughly constant over a broader frequency range. An equivalent time-domain interpretation may be provided by considering the step response. The inductor delays current flowing through the branch containing the resistor, making more current available for charging the capacitor, reducing the rise-time, thus extend the bandwidth. The transfer function of the shunt inductive peaking circuit is

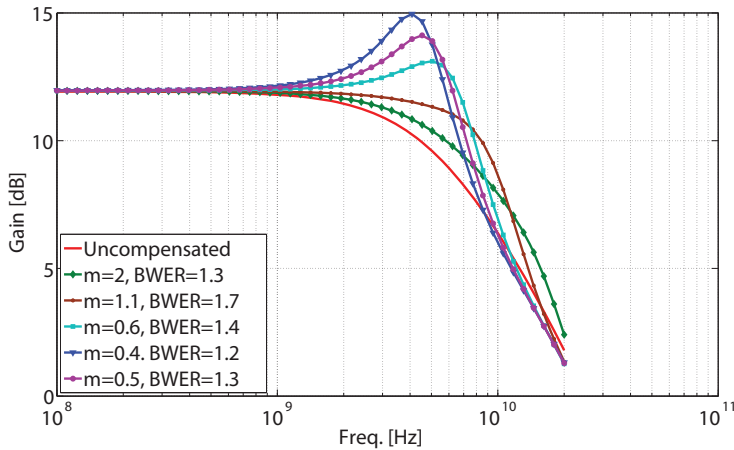
$$Z(s) = \frac{V_{out}}{I_{in}} = \frac{R + sL}{1 + sRC + s^2LC} \quad (4.3)$$

Introducing a factor  $m$ , defined as the ratio of the  $RC$  and time constants  $L/R$

$$m = \frac{RC}{L/R} = \frac{R^2C}{L} \quad (4.4)$$

As can be seen, the inductor introduces a zero in  $Z(s)$  that increases the impedance with frequency compensating the decreasing impedance of the capacitor  $C$ . The addition of a zero improves the bandwidth but also peaks the response. Fig. 4.26 shows the bandwidth improvement with several values of the inductor. For ideal components, the maximized bandwidth occurs at a value of  $m = \sqrt{2} \approx 1.41$ , which extends the bandwidth to a value about 1.85 times as large as the uncompensated bandwidth. Besides, a maximum flat gain is achieved for  $m = 1 + \sqrt{2} \approx 2.41$





**Figure 4.26:** Bandwidth improvement with shunt peaking.

although the bandwidth extension ratio (BWER) is reduced to 1.72 [59]. However, for the real RF components provided by TSMC on 90 nm low-power process, simulation results show that  $m = 1.1$  give the maximum BWER of 1.7 with no peaking. Shunt peaking technique was widely employed in many designs such as [60] - [62].

### Series peaking

Series peaking is a bandwidth extension technique in which the parasitic capacitors  $C_1$  and  $C_2$  are separated by an inductor as depicted in Fig. 4.27. A series inductor  $L$  across  $R$  and  $C$  is used to create a series peaking in the frequency response. The series inductor creates a second-order  $RLC$  resonant circuit with a resonance frequency  $\omega_0 = 1/\sqrt{LC}$ . The transfer function of the series inductive peaking circuit is

$$Z(s) = \frac{V_{out}}{I_{in}} = \frac{R}{1 + sRC + s^2LC} \quad (4.5)$$

where  $m$  as defined above determines the pole locations and the overdamped response of the amplifier. As the value of  $m$  increases poles become complex conjugate and travel along the real axis towards the  $j\omega$  axis. The circuits with more than two reactance components have more than one resonance mode. A multi-resonance circuit can be utilized to cover a wider frequency range than a single resonance circuit. For this reason, the resonance frequencies should be chosen properly to optimize the bandwidth of interest [63]. By series inductive peaking, the bandwidth is further increased as demonstrated in Fig. 4.28. Inductive series peaking technique was utilized in [64] [65].

### T-coil peaking

A bandwidth extension method that offers a greater BWER is a combination of shunt and double series peaking called T-coil peaking. In this technique the parasitic capacitors of the transistors

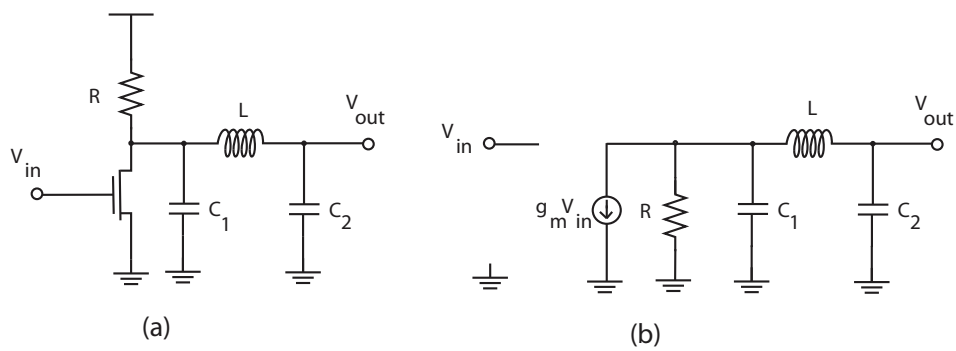


Figure 4.27: (a) A common-source amplifier with series peaking. (b) Equivalent small-signal model.

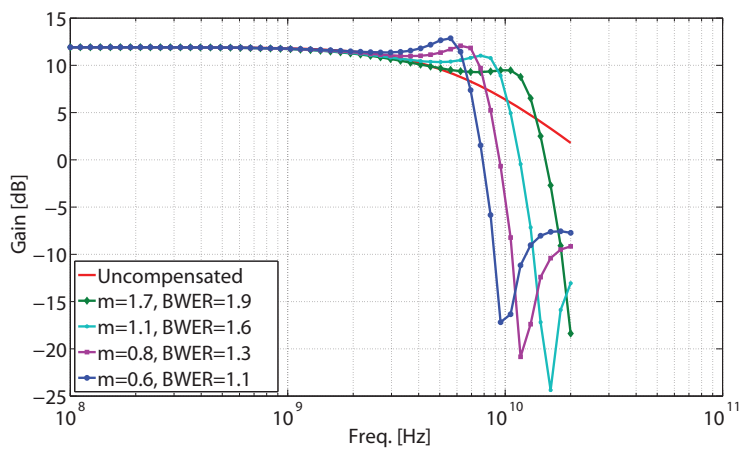
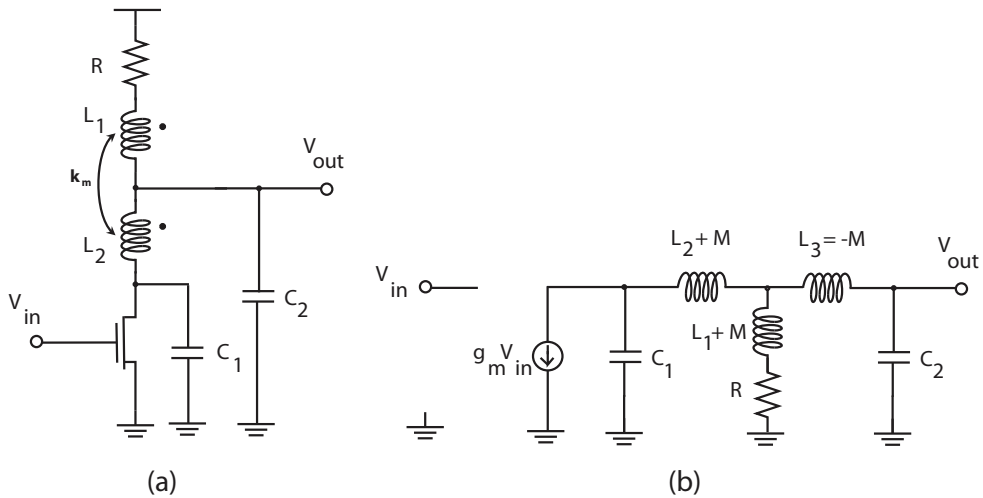


Figure 4.28: Bandwidth improvement with series peaking.



**Figure 4.29:** (a) A common-source amplifier with T-coil peaking. (b) Equivalent small-signal model.

and inherent mutual inductance of the inductors are taken as a part of the design. A common-source amplifier with T-coil peaking is shown in Fig. 4.29. The mutual coupling,  $M$  forms a third inductor  $L_3$ . The magnetic coupling coefficient,  $k_m = M/\sqrt{L_1 L_2}$  between  $L_1$  and  $L_2$  can be exploited to modify the bandwidth extension. The flow of current into the load resistor continues to be deferred by the action of  $L_1$ . In addition, the inductor  $L_2$  delays the diversion of current into the rest of the network. Some time after the drain voltage has risen significantly, the voltage across the load capacitance begins to rise as current finally starts to flow through  $L_3$ . Hence, such a network charges the capacitances serially in time rather than in parallel. The trade-off is an increased delay in exchange for the improved bandwidth [59].

The factor  $m_1, m_2$  are defined as follows:  $m_1 = R^2 C/L_1$ ,  $m_2 = R^2 C/L_2$ . Fig. 4.30 plots bandwidth improvements for various values of the T-coil. T-coil peaking technique was successfully applied in [63] [66] - [68].

#### 4.4.2 Proposed Quantizer

The proposed quantizer is shown in Fig. 4.31 [Paper VII]. For a differential quantizer, the differential threshold voltages are achieved by using an inverting amplifier with unity gain as shown in the figure. The core of the quantizer is a UWB high-gain differential amplifier. A very high gain is required for high input sensitivity quantization, thus a very small signal can be detected. Due to the gain-bandwidth trade-off, wider bandwidth is achieved at the expense of lower gain per stage. In order to recover the gain, a cascade of six differential amplifiers is used as shown in Fig. 4.32. For bandwidth enhancement, the T-coil peaking and shunt peaking are chosen in this design. T-coil peaking technique gives the largest bandwidth extension factor among the aforementioned techniques while the shunt peaking can provide optimal group delay. The T-coil peaking is applied for the first amplifying stage to form the desired bandwidth. Bandwidth is extended significantly with a trade-off in creating a peaking in the frequency response. The

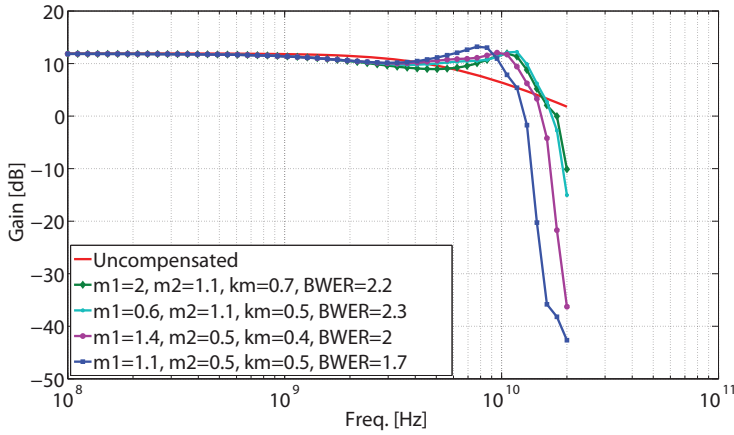


Figure 4.30: Bandwidth improvement with T-coil peaking.

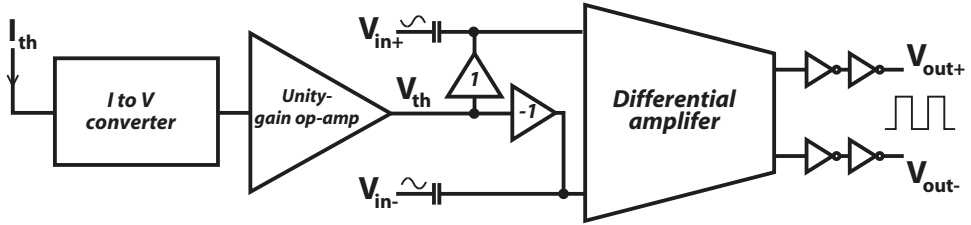
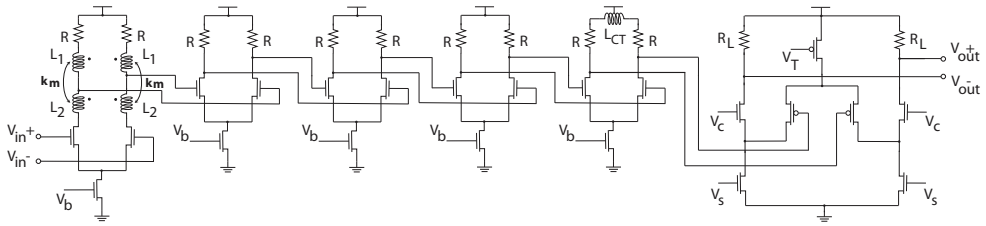
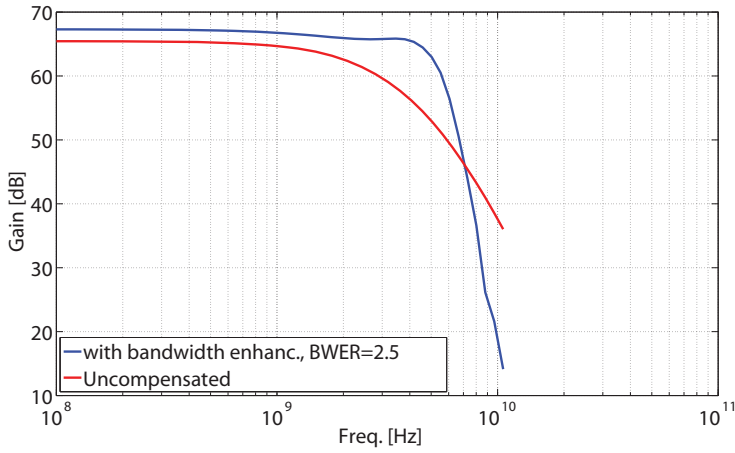


Figure 4.31: The proposed differential quantizer.

peaking is designed to be located at the roll-off frequency band of the next three amplifying stages. As the result, the peaking will be suppressed without an additional bridge-capacitor as exploited in [57]. A shunt peaking using a center-tap inductor is applied for the fifth amplifying stage to further extend the bandwidth as well as obtain a flat gain response. The T-coil and the center-tap inductor are designed and optimized by Advanced Design System 2009 (ADS2009). The two top metal layers are used to increase the series inductance of the inductor. The S-parameters were extracted from electromagnetic field simulation and then imported into Cadence for post-layout simulation. The stacked structure is proposed for the T-coil to provide the best area efficiency, the highest self-inductance and the highest coupling,  $k_m = 0.9$ . Both T-coil and center-tap inductor have metal width of  $10 \mu\text{m}$ , metal spacing of  $2 \mu\text{m}$  and inner radius of  $30 \mu\text{m}$ . They achieve the inductances of approximately  $9.5 \text{ nH}$  and a peak quality factor of 5 over the designed bandwidth of  $0\text{--}5 \text{ GHz}$ . The output amplifying stage of the differential quantizer is a fully-differential folded cascode amplifier with a high gain of more than  $20 \text{ dB}$  and fast settling response. The folded cascode with the pMOS input pair limits the lower voltage swing allowing the upper voltage swing can reach  $V_{DD}$ . The gain of this folded cascode differential amplifier can be tunable by changing the tail current as well as changing the current 'folded' up through the load resistors. Each output of the quantizer is buffered by cascaded inverters.



**Figure 4.32:** The proposed high-gain, ultra-wideband differential amplifier.



**Figure 4.33:** The simulated gain response of the differential amplifier.

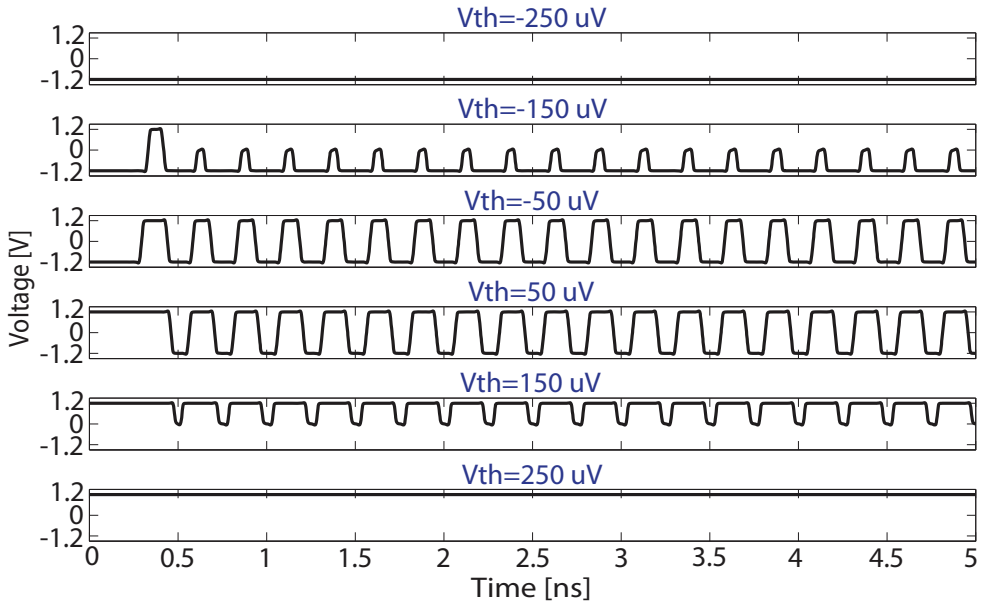
### 4.4.3 Post-Layout Simulation Results

Post-layout simulation results of the quantizer for TSMC 90 nm CMOS technology is achieved using the Cadence design environment. All components used for simulation are RF models provided by TSMC. Fig. 4.33 shows the gain response of the differential amplifier. A high differential gain of approximately 70 dB over the -3 dB bandwidth from near DC to 5 GHz, is demonstrated. The bandwidth is improved by 2.5 times the uncompensated bandwidth. Table 4.3 gives a comparison of some reported designs. In [71] distributed architecture is employed to extend the bandwidth trading off against increases in die area and power dissipation. Transformers are used in [72] as passive matching circuits combined with neutralization technique allowing this filter suitable for W-band applications.

Fig. 4.34 gives the performance of the quantizer when differential sinusoidal signals are applied at the input for some threshold levels. The input signals have the amplitude of 1 mV peak to peak, frequency of 4 GHz. The differential threshold voltages are swept with the step size of 100  $\mu$ V. Swept threshold can be used when the received signal is significantly above the noise floor. With a high threshold, the signal pulse width can vary depending on where the threshold will hit the incoming signal and hence can have shorter pulses into the system. Stochastic resonance technique [5] can be used when the received strength is very weak and almost buried in the noise floor. The threshold can be set to the signal average value so that the

**Table 4.3:** Comparison with previous published differential amplifiers

Ref.	CMOS tech.	Power cons. (mW)	Topology	Gain (dB)	-3 dB BW (GHz)	Unity-gain BW (GHz)	No. of stages
[69]	0.18 $\mu$ m	3.8	Diff. folded cascode	63.12	–	2	1
[70]	65 nm	10.17	Diff.	84	–	0.2	3
[71]	0.6 $\mu$ m	216	Diff. distributed	5.5	–	8.5	4
[72]	90 nm	94	Diff.	11	93–104	–	6
This work	90 nm	33.5	Diff. + folded cascode	70	0–5	11.8	6



**Figure 4.34:** The simulated performance of the proposed differential quantizer when the differential threshold voltages are swept.

weak signals are amplified above the noise floor and are detected.

**4.4.4 Summary**

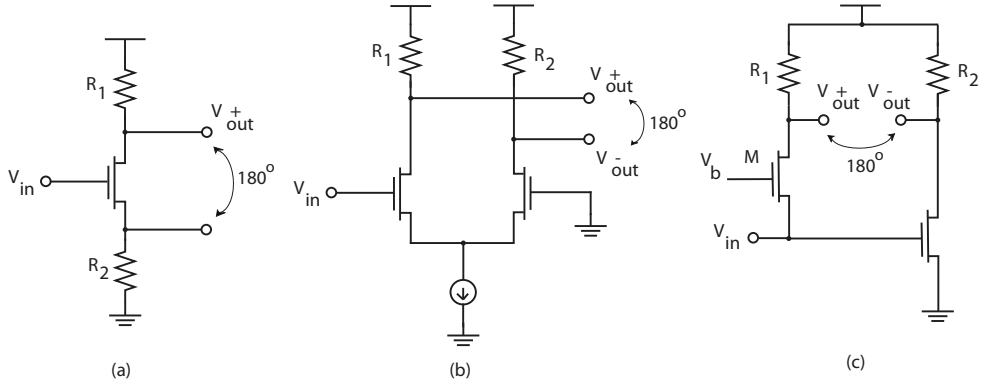
We have presented an ultra-wideband, differential, single-bit quantizer intended for IR-UWB applications [Paper VII]. The proposed quantizer is working in continuous-time for power-efficient IR-UWB implementations with a 5 GHz bandwidth and a very high differential gain of approximately 70 dB while consuming 33.5 mW from a 1.2 V supply voltage. Coupled inductors are explored for bandwidth extension and post-layout simulation results are provided.

## 4.5 Proposed UWB Differential Quantizer Exploiting Noise Cancellation

Since input signal from the antenna is usually single-ended, conversion to a differential signal is required. Some designers use off-chip baluns to generate differential signals. However, the external balun increases system cost and causes extra gain and NF degeneration of about 1 dB or even more. To handle this problem, an on-chip active balun is employed to achieve single-end to differential conversion. Using of an active balun can avoid the requirement of an off-chip passive one for differential signaling in wireless receivers, leading to a low-cost and low-power chip solution.

### 4.5.1 Active Balun Topologies

Several active balun topologies have been proposed in the literature. The simplest active balun is a common source based stage with resistors at the drain and the source as depicted in Fig. 4.35a. With the signal input to the gate, ideally the signal at the drain will be phase shifted by  $180^\circ$  relative to the signal at the source. Besides, by properly choosing the value of these resistors, the amplitude of the two outputs can be made equal. However, this circuit becomes unsuitable for high frequency applications due to the parasitic elements associated with the transistor. In particular, the gate-drain parasitic capacitance,  $C_{gd}$  seriously degrades the performance at high frequencies since the input signal can feed through this capacitance directly to the output. Two techniques that have better performance are the differential pair and the cascaded common-gate/common-source (CG/CS) stage as shown in Fig. 4.35b and Fig. 4.35c, respectively. Consisting of a differential pair stage with one of the two inputs grounded, the RF signal applied to the other input, is capable of providing high gain and ideally split equally between the output pair. In ideal conditions, it provides  $180^\circ$  phase shift between the two output signals. An important advantage of differential operation over single-ended signaling is higher immunity to noise. Another useful property is the increase in maximum achievable voltage swings. However, the differential pair circuit ultimately has a similar frequency limitation as the circuit in Fig. 4.35a by considering the parasitics in the half-equivalent circuit. In addition, as reported in [73], the impedance of a non-ideal current source is not as high as required, resulting in unequal signal distribution, thereby leading to imbalance in the differential output. A viable solution may be active balun based on a parallel configuration of CG and CS stages explored in low noise amplifiers. It can simultaneously provide wideband input matching and relatively low noise figure [74] [75]. It is desirable to have a low input reflection coefficient so the input power will not be reflected. Since the input impedance to the gate of a MOSFET is typically very high, the reflection coefficient to a CS stage or differential pair is generally poor. In contrast, the input impedance to a CG stage is approximately  $1/g_m$ . Since the input impedance of the CG stage is in parallel to the very high input impedance of the CS stage, the total input impedance is approximately of that of CG stage. Therefore, an appropriate selection of device size and biasing can provide  $50\ \Omega$  input impedance, as desired.



**Figure 4.35:** (a) CS-based balun, (b) Differential pair as balun, (c) Cascaded CG/CS balun.

## 4.5.2 Proposed Quantizer

The proposed quantizer exploits an active balun at the input to obtain single-ended to differential conversion as well as to cancel the thermal noise of the input matching device as shown in Fig. 4.36. The CG stage has a straightforward relation between its voltage gain  $A_{V,M1}$  and its input impedance  $R_{in,CG}$ . The signal current flowing through the load resistor  $R_{CG}$  has to be equal to the one flowing at the input  $i_{in}$ . Thus,

$$i_{in} = \frac{V_Y}{R_{CG}} = \frac{v_{in} \cdot A_{V,M1}}{R_{CG}} \quad (4.6)$$

As a result, the input impedance of the CG stage can be expressed as

$$R_{in,CG} = \frac{v_{in}}{i_{in}} = \frac{R_{CG}}{A_{V,M1}} \quad (4.7)$$

For an idea transistor, having infinite output resistance, this is obvious. In that case the input impedance can be written as  $R_{in,CG} = 1/g_{m1}$  and the gain equals  $A_{V,CG} = g_{m1} \cdot R_{CG}$ . However, (4.6) and (4.7) are equally valid when the finite output resistance and body-effect of a real transistor are taken into account.

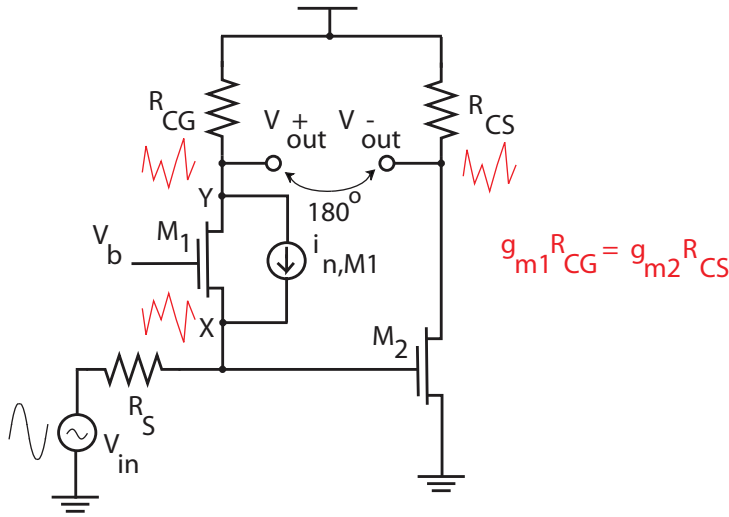
For an impedance matching at the input, the input impedance of the CG stage should equal the source resistance. Thus, the gain of the CG stage becomes:

$$A_{V,CG} = \frac{R_{CG}}{R_{in,CG}} = \frac{R_{CG}}{R_S} \quad (4.8)$$

To create a balun, the gain of the CS stage should be equal to the gain of the CG stage in amplitude, but has opposite sign, thus

$$A_{V,CS} = -A_{V,CG} = -\frac{R_{CG}}{R_S} \quad (4.9)$$





**Figure 4.36:** An active balun based on CG and CS stages (bias now shown).

Noise cancellation of matched devices can be achieved by noise inversion and subtraction. The noise current of  $M_1$  which is modeled by the current source  $I_{n,M1}$ , flows into node X but out of node Y. This creates two fully correlated noise voltages at node X and Y with opposite phases as depicted in Fig. 4.36. On the other hand, the signal voltages at nodes X and Y are in phase. The difference in sign for noise and signal makes it possible to cancel the noise of the matching device while simultaneously adding the signal contributions constructively. By properly designing  $g_{m1}$  and  $g_{m2}$ , the noise contributed by  $M_1$  can be cancelled at the output by subtraction. The condition for complete noise cancellation is derived as:

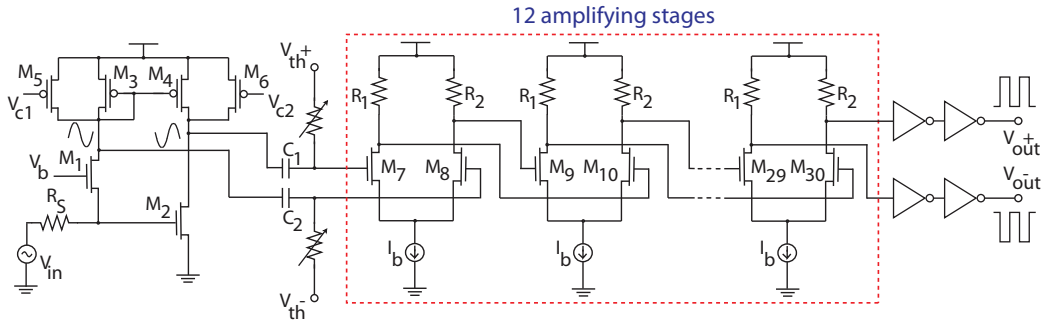
$$g_{m1} \cdot R_{CG} = g_{m2} \cdot R_{CS} \quad (4.10)$$

When the input is matched, the NF can be calculated by the following equation:

$$NF = 1 + \frac{R_S}{R_{CG}} + \gamma \frac{R_{CS}}{R_{CG}} + \frac{R_S \cdot R_{CS}}{R_{CG}^2} \quad (4.11)$$

where  $R_S$  is source impedance,  $\gamma$  is the excess noise coefficient. The gain required for noise cancellation equals the gain required to obtain balun operation, leading to the conclusion that simultaneous balancing and noise cancellation of the impedance matching device is possible. Besides, the same mechanism leading to cancellation of the output noise due to the matching device can also be exploited to cancel its distortion components as derived in [76]. As a result, not only the noise of the CG stage is cancelled but also its nonlinearity. However, since the parallel configuration of the CG and CS stages can be considered as a two-stage circuit, it consumes more power compared to single-stage circuit. The power consumption can be reduced by sharing the same bias current for the CG and CS stages as exploited in [77].

The proposed quantizer is shown in Fig. 4.37 where the first stage is an active balun. Transis-



**Figure 4.37:** The proposed continuous-time differential single-bit quantizer.

tors  $M_5$  and  $M_6$  perform gain variation by means of current steering. The goal is to compensate for amplitude mismatch of the differential signals at the output of the active balun. The current steering technique is favourable especially for low-noise amplifiers as the noise generated by the gain-control transistors has a relatively low effect on the overall NF compared to other approaches. When the gate of  $M_5/M_6$  is connected to a lower voltage, the transconductance of  $M_3/M_4$  is reduced as a result of smaller current, thus leading to a lower gain. Due to the gain-bandwidth trade-off, wider bandwidth is achieved at the expense of lower gain per stage. In order to recover gain, a cascade of twelve fully-differential amplifiers is employed after the balun. The threshold voltages are added with the differential signals at the amplifiers' inputs providing controllable quantization voltage levels for input signal thresholding. The outputs of the quantizer are buffered by cascaded inverters.

### 4.5.3 Measurement Results

In order to verify the performance of the differential quantizer, a chip prototype was implemented in 90 nm CMOS provided by TSMC [Paper III]. The quantizer core occupies a die area of  $0.68 \times 0.14 \text{ mm}^2$  as shown in Fig. 4.38. For measurement, fabricated dies were bonded directly to Rogers PCBs to avoid the inductive load of a package and to avoid long bond wires. Input RF interface was connected to a SMA connector. Adopted  $50 \Omega$  transmission line, the RF signal path was carefully designed and isolated. The transmission line is located as close as possible to the high frequency input pad to reduce the length of bond wire as well as the parasitic series inductance. The outputs of the balun and differential quantizer were measured by means of on-chip probing. The probe pads were designed for ground-signal-ground-signal-ground (GSGSG) dual-signal probes with  $100 \mu\text{m}$  pitch. Measurements were performed with a LeCroy Wavemaster 830Zi oscilloscope, a Rohde & Schwarz FSQ26 signal analyzer and a Signatone WL-170-6 Wavelink RF probe station. The measurement setup for the quantizer is shown in Fig. 4.39.

Measurement results of the active balun show that the gain imbalance remains within  $\pm 1 \text{ dB}$  from 250 MHz to 7 GHz and the phase imbalance is within  $\pm 5^\circ$  between 200 MHz and 5 GHz as plotted in Fig. 4.40. Fig. 4.41 shows the gain response of the differential quantizer. It obtains a differential peak gain of 35 dB around 1 GHz while the -3 dB bandwidth is from 100 MHz to

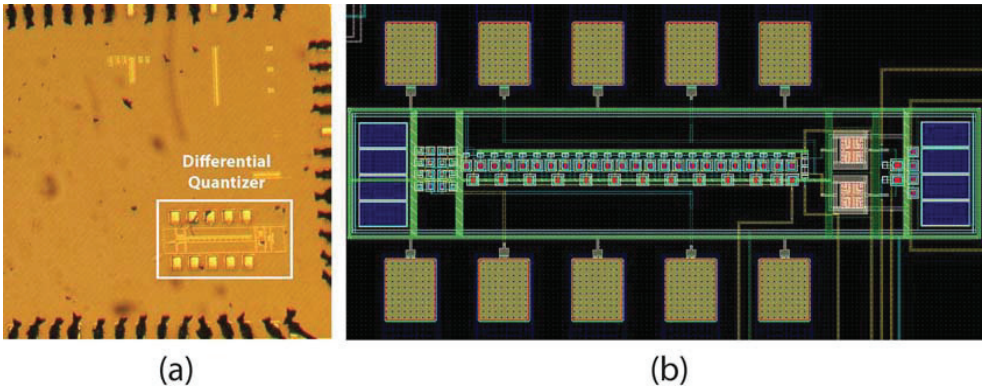


Figure 4.38: The die microphotograph (a) and the layout (b) of the proposed differential quantizer.

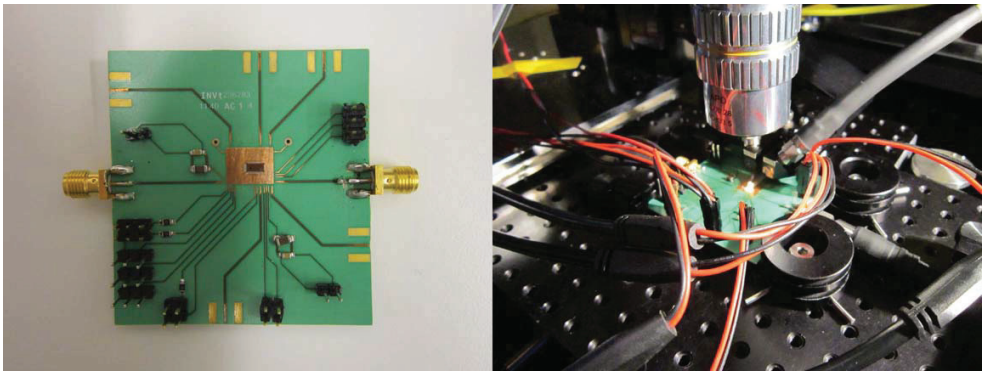


Figure 4.39: The measurement setup for the differential quantizer.

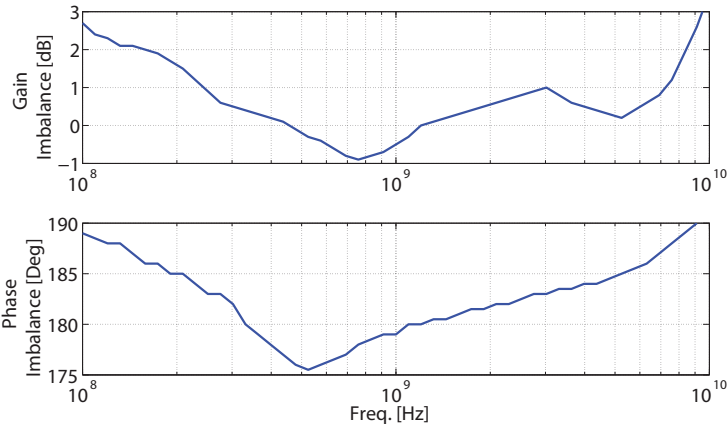
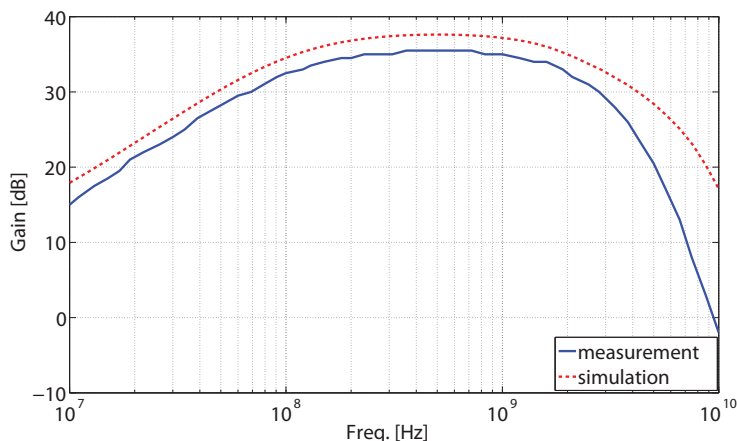


Figure 4.40: The measured gain imbalance and phase imbalance of the balun.



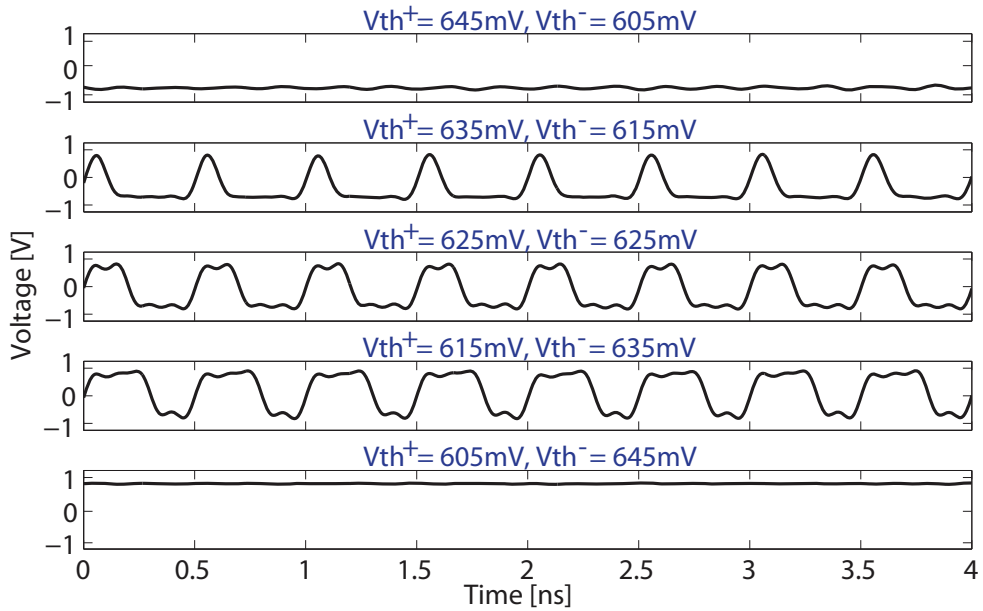
**Figure 4.41:** The measured and simulated differential gain response of the proposed quantizer.

**Table 4.4:** Comparison with previous published single-bit comparators

Ref.	CMOS tech.	Die area mm <sup>2</sup>	Power cons. (mW)	Sensitivity (mV)
[43]	0.11 $\mu$ m	0.08	37*	—
[44]	0.12 $\mu$ m	0.48	2.65*	29.4@5 GHz
[45]	65 nm	0.16	1.3*	27.2@5 GHz
[78]	90 nm	0.04	4.8	45@2 GHz
This work	90 nm	0.09	13.1	40@2 GHz

\* w/o clock

2.5 GHz. At frequencies beyond 3 GHz, the measured gain response differs from the simulated one. This is probably due to bond wire inductances combined with parasitic capacitances limiting the bandwidth as well as changing the high-frequency impedance matching. Fig. 4.42 gives the performance of the quantizer when a sinusoidal signal is applied at the input for some threshold levels. At 2 GHz the quantizer can detect a signal with minimum amplitude of 40 mV peak to peak. The differential threshold voltages are swept with the step size of 10 mV. The quantizer consumes 13.1 mW from a 1.2 V supply voltage. Table 4.4 compares the proposed quantizer to previous published single-bit comparators/quantizers in CMOS. In [43], a 10 GHz 3-stage comparator in 1.2 V 0.11  $\mu$ m CMOS is presented and is designed to extract every 4<sup>th</sup> bit of a 40 Gb/s data stream. A bit error rate less than  $10^{-12}$  for 1 V peak to peak at the input is achieved. The comparator in [44] reaches a sensitivity of 29.4 mV at 5 GHz. In [45], a comparator with similar circuit structure as used in [44] is described. It obtains a sensitivity of 15 mV at 3 GHz and 27.2 mV at 5 GHz. Again, the sensitivity here is defined as the weakest pulse signal level that can be detected by the comparators.



**Figure 4.42:** The measured performance of the proposed differential quantizer when the differential threshold voltages are swept.

#### 4.5.4 Summary

We have proposed a power-efficient continuous-time differential single-bit quantizer intended for IR-UWB receivers [Paper III]. It exploits an input active balun to obtain single-ended to differential conversion. The quantizer prototype was fabricated in 90 nm CMOS and occupies a chip area of 0.09 mm<sup>2</sup>. The proposed quantizer achieves a -3 dB bandwidth of 2.4 GHz with a high differential gain of 35 dB and a sensitivity of 40 mV at 2 GHz. Power consumption is 13.1 mW from a 1.2 V supply voltage. The quantizer is compact and can be fully integrated without any external clock reference.

## 4.6 Conclusion

A different approach for IR-UWB radio named Continuous-Time Binary-Value (CTBV) signal processing have been proposed. By avoiding clocks, power efficient solutions are feasible in standard CMOS. In this chapter, four different single-bit quantizers have been demonstrated in 90 nm CMOS [Paper III][Paper IV][Paper VII][Paper IX]. By exploiting the relaxed linearity requirement, other critical parameters such as gain and noise can be improved significantly. The advantages of analog thresholding using single-bit quantizer are as follow. Firstly, it is best suited for receivers with low SNR. Secondly, optimal threshold value can be estimated using different options such as swept thresholding or stochastic resonance.



# Chapter 5

## UWB LOW NOISE AMPLIFIERS AND MIXERS

### 5.1 Low Noise Amplifiers

#### 5.1.1 Introduction

One of the major challenges in designing a wideband communication system is the design of a wideband low noise amplifier (LNA). The LNA serves as the first active building block of the wireless receiver. It amplifies the incoming signal without adding much noise and distortion. The noise performance of the LNA significantly influences the overall system noise performance. Furthermore, the LNA must provide wideband on-chip input matching to a  $50\ \Omega$  antenna, some filtering of out-of-band interferers and good linearity while consuming low power. The wideband LNA designs can be classified as distributed amplifiers (DAs), resistive/reactive feedback amplifiers, BPF-based amplifiers and noise-cancelling amplifiers. Each topology has distinct advantages and limitations. DAs utilize several parallel transistors and artificial transmission lines to periodically combine the gain of each stage on the output line [79] - [83]. The overall gains of DAs depend linearly on the number of stages. This topology offers wideband characteristics, flat gain and high linearity. However, CMOS DAs often tend to be power hungry and consume large chip areas. Alternatively, the feedback amplifier topology provides wideband input matching and flat gain. Among the feedback approaches, the resistive feedback is an area-saving solution that proves to be appropriate for the implementation of the input matching in the 3-5 GHz UWB band. Many variations of wideband resistive feedback LNAs have been implemented [84] - [88]. A resistive feedback offers higher stability and gain bandwidth enhancement. However, the noise performance is limited. Whereas, an UWB reactive feedback implementation provides better noise performance and an increase in linearity trading increase of die area [89] [90]. Another popular wideband topology of interest is the filter-based amplifier that utilize Butterworth or Chebyshev BPFs for the input impedance matching network [91] [92]. The BPF-based topology incorporates the input impedance of the conventional narrowband cascode amplifier as a part of the filter. These filters have demonstrated excellent input impedance matching, power consumption and gain across a wide frequency range [93]. However, the use of

the filter at the input required a number of additional reactive elements which inevitably resulted in larger chip area when implemented on-chip or the additional external components. Besides, the input filter insertion loss degrades the LNA's NF. Noise cancelling is an effective approach for achieving a low NF and an impedance matching simultaneously without the need for large inductors or feedback. The feedforward noise-cancelling technique was proposed to break the tradeoff between noise factor and input impedance matching [94] - [96]. In this section, we propose a LNA exploring both low input impedance of common gate LNA and noise cancellation technique to improve the performance of a UWB LNA [Paper II].

### 5.1.2 Noise

Noise is the random fluctuation of electrical power that interferes with the desired signal. It limits the minimum signal level that a circuit can process with acceptable quality. Especially, integrated chip solutions using modern technology must treat noise because it trades with power dissipation, speed and linearity. There are various noise sources, but probably the most common are thermal noise and flicker noise. These two noise have been taken into account in the design of the proposed LNA in this chapter.

#### Thermal Noise

Thermal noise is a consequence of Brownian motion in which thermally agitated charge carrier in a conductor constitutes a randomly varying current that gives rise to a random voltage [59]. Since the noise process is random, it is not possible to assign a particular voltage at a certain time, thus a statistical approach has to be adopted to characterize the noise, such as the mean square or root-mean-square values. For example, the mean-square open-circuit noise voltage generated by a resistor  $R$  can be calculated as

$$\overline{e_n^2} = 4kTR\Delta f \quad (5.1)$$

where  $k$  is Boltzman constant (about  $1.38 \times 10^{-23}$  J/K),  $T$  is the absolute temperature in Kelvin and  $\Delta f$  is the noise bandwidth in hertz. The dependence of thermal noise upon  $T$  suggests that low-temperature operation can decrease the noise in analog circuit.

MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. In the triode region of operation particularly, noise is proportional to the resistance value. Indeed, detailed theoretical considerations lead to the following expression for the drain current noise of MOSFETs

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad (5.2)$$

where  $g_{d0}$  is the channel conductance for  $V_{DS} = 0$  and  $\gamma$  is a noise parameter. For long-channel devices,  $\gamma$  equals to unity when the MOSFET operates in triode region and equals to 2/3 in the saturation region. For short-channel devices,  $\gamma$  exceeds unity in saturation and may become 2-3 under some biasing conditions. The ohmic sections of a MOSFET also contribute thermal noise. The gate, source and drain materials exhibit finite resistivity, thereby introducing noise. For a relatively wide transistor, the source and drain resistance is typically negligible whereas



the gate distributed resistance may become noticeable. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. Although this noise is negligible at low frequencies, it can dominate at radio frequencies. It is shown that the gate noise may be expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \quad (5.3)$$

where  $\delta$  is the gate noise coefficient. For long-channel devices,  $\delta$  equals to  $4/3$ . The parameter  $g_g$  is

$$g_g = \frac{w^2 C_{gs}^2}{5g_{d0}} \quad (5.4)$$

### Flicker Noise

Flicker noise is a general term used to describe a family of effects which produce a  $1/f$  spectrum.  $1/f$  noise dominates the noise spectrum at low frequency in most conducting materials and a wide variety of semiconductor devices. In semiconductor devices,  $1/f$  noise is most prominent in devices that are sensitive to surface phenomena. Hence, MOSFETs exhibit significantly more  $1/f$  noise than do bipolar devices. The sources of  $1/f$  noise in MOS transistors are mainly by the fluctuations of the channel free carriers due to the random trapping and detrapping of charges in the oxide traps near the  $Si$  and  $SiO_2$  interface.

The mean-square  $1/f$  drain noise current is given by

$$\overline{i_n^2} = \frac{K}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \quad (5.5)$$

where  $K$  is a process-dependent constant on the order of  $10^{-25} V^2 F$ . The flicker noise does not depend on the bias current or the temperature. The inverse dependence of noise current on  $WL$  suggests that to decrease  $1/f$  noise, the device size must be increased. It is also experimentally verified that PMOS devices exhibit less  $1/f$  noise than NMOS transistors because the former carry the holes in a "buried channel" [97].

### Noise Factor, Noise Figure and Noise Temperature

A useful measure of the noise performance of a system is the noise factor, usually denoted as  $F$ . The noise factor is defined as

$$F \equiv \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad (5.6)$$

where the source is at temperature of 290 K. The noise factor is a measure of the degradation in signal-to-noise ratio that a system introduces. The larger the degradation is, the larger the noise factor. If a system adds no noise of its own then the total output noise is due entirely to the source and the noise factor is therefore unity. In addition to noise factor, other figures of merit that often crop up in the literature are noise figure and noise temperature. The noise figure (NF)

is simply the noise factor expressed in decibels.

$$NF = 10\log_{10}F \quad (5.7)$$

Noise temperature,  $T_N$  is an alternately way of expressing the effect of an amplifier's noise contribution and is defined as the increase in temperature required of the source resistance for it to account for all of the output noise at the reference temperature  $T_{\text{ref}}$  (which is 290 K). It is related to the noise factor as follows

$$F = 1 + \frac{T_N}{T_{\text{ref}}} \Rightarrow T_N = T_{\text{ref}}(F - 1) \quad (5.8)$$

An amplifier that adds no noise of its own has a noise temperature of zero Kelvin.

### 5.1.3 Input Architecture of LNAs

State-of-the-art CMOS UWB LNAs employ various techniques to simultaneously achieve wideband gain and matching. In the following, some of the most popular wideband LNA topologies in the literature are reviewed briefly, highlighting advantages and drawbacks within the actual UWB systems [98].

#### Common Source LNA with Resistive Termination

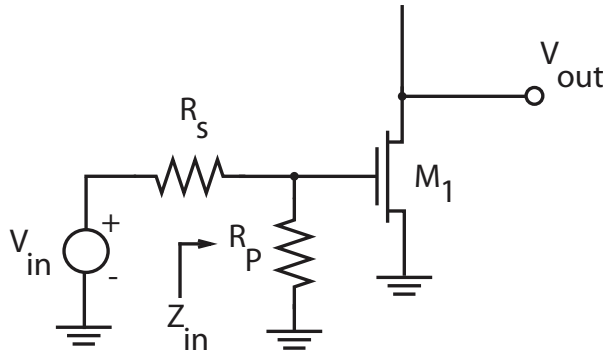
In this technique, a  $50 \Omega$  resistor is placed in parallel with the input and the capacitive part of the input impedance is cancelled by an external inductor to provide  $50 \Omega$  input impedance as shown in Fig. 5.1. However, this termination resistor generates noise. The noise factor of the circuit can be calculated as

$$F = \frac{\overline{V_{n,\text{Out}}^2}}{\overline{V_{n,\text{Rs}}^2}} = \frac{\overline{V_{n,\text{Rs}}^2} + \overline{V_{n,\text{Rp}}^2} + \overline{V_{n,\text{M1}}^2}}{\overline{V_{n,\text{Rs}}^2}} \approx \frac{4kT(R_S//R_P)\Delta f \cdot g_m^2 R_D^2 + \overline{i_{nd}^2} R_D^2}{4kT R_S \Delta f \cdot 1/4g_m^2 R_D^2} \quad (5.9)$$

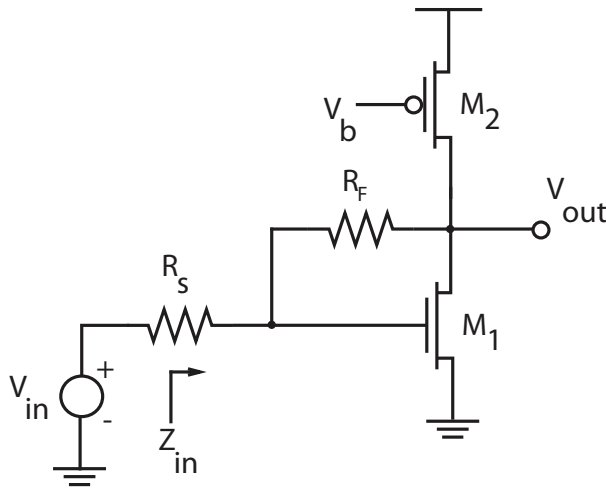
where  $\overline{V_{n,\text{Out}}^2}$  represents the total output noise;  $\overline{V_{n,\text{Rs}}^2}$ ,  $\overline{V_{n,\text{Rp}}^2}$  and  $\overline{V_{n,\text{M1}}^2}$  are the output noise due to  $R_S$ ,  $R_P$  and  $M_1$ , respectively;  $R_D$  is the load resistance at the drain of  $M_1$ ;  $k$  is the Boltzmann's constant and  $T$  is the absolute temperature. The MOSFET  $M_1$  has various noise sources. However, for simplicity, only the channel thermal noise is taken into account as it is the dominant noise source in most conditions. Equation can be further simplified to

$$F = \frac{4(R_S//R_P)}{R_S} + \frac{4\gamma}{\alpha g_m R_S} = 2 + \frac{4\gamma}{\alpha g_m R_S} \quad (5.10)$$

where  $\alpha = g_m/g_{d0}$  is typically less than one,  $g_{d0}$  is the channel conductance for  $V_{DS} = 0$  and  $\gamma$  is a noise parameter. For long-channel devices,  $\gamma$  equals to unity when the MOSFET operates in triode region and equals to 2/3 in the saturation region. For short-channel devices,  $\gamma$  can be significantly larger than 2/3. Thus, noise figure of this architecture can be much larger than 3 dB. The poor noise figure makes this architecture unattractive for applications where low NFs as well as good input matchings are desired.



**Figure 5.1:** Common source LNA with resistive termination.



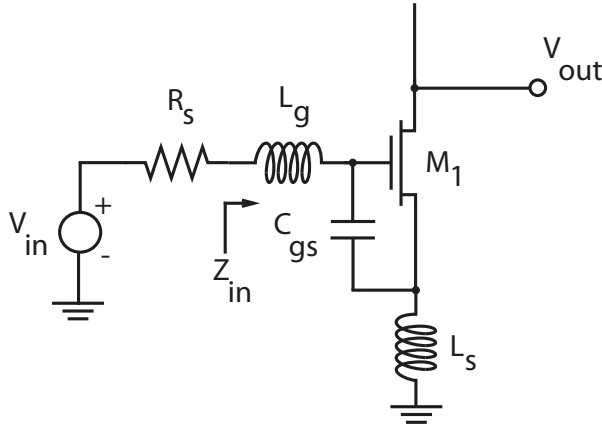
**Figure 5.2:** Common source LNA with resistive shunt feedback.

### Common Source LNA with Resistive Shunt Feedback

The circuit topology of a resistive shunt feedback LNA (RFLNA) is shown in Fig. 5.2.  $M_2$  operates as a current source and  $R_F$  senses the output voltage and returns a current to the input.  $R_F$  is determined by the input impedance matching as

$$Z_{in} = R_F / (1 + |A_V|) \quad (5.11)$$

where  $A_V$  is the voltage gain of the common-source amplifier. The RFLNA provides wideband input and output matching and small die area because no inductor is required for input matching. However, it has a poor NF and consumes a large amount of power. The additional noise coming from  $R_F$  is one of the main limitations of this topology. When  $M_1$  is increased to reduce NF, it requires a shunt inductor to improve input matching [99]. This topology is sensitive to process variations as the input impedance  $Z_{in}$  is dependent on  $R_F$  and  $A_V$ . In addition, the total phase



**Figure 5.3:** Common source LNA with source inductive degeneration.

shift around the loop may create instability for certain source and load impedances. The noise factor can be calculated as

$$F = 1 + \frac{4R_s}{R_F} + \gamma + \gamma g_{m2} R_s \quad (5.12)$$

For  $\gamma \approx 1$ , the NF exceeds 3 dB even if  $4R_s/R_F + \gamma g_{m2} R_s \ll 1$ .

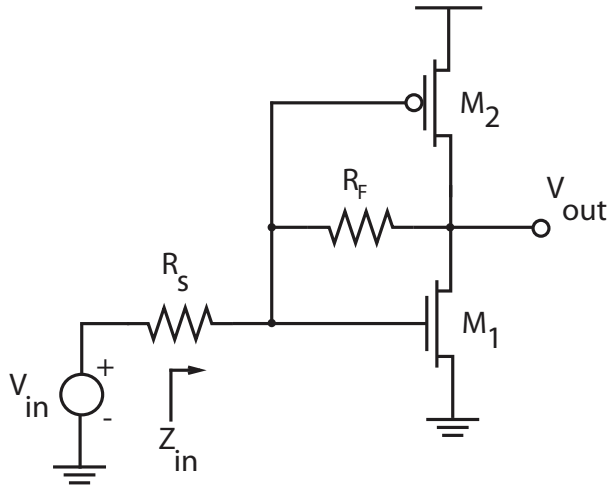
### Common Source LNA with Source Inductive Degeneration

Fig. 5.3 shows a typical inductively degenerated common-source LNA (L-CSLNA). This architecture employs source inductive degeneration to generate a real term in the input impedance. The input impedance is

$$Z_{in} \approx j \left\{ \omega L_g + \omega L_s - \frac{1}{\omega C_{gs}} \right\} + (g_{m1}/C_{gs}) L_s \quad (5.13)$$

where  $C_{gs}$  is the parasitic gate-to-source capacitance. This equation suggests that the resistive term is directly proportional to the inductance value. Whatever value this resistive term is, it does not generate thermal noise since a pure reactance is noiseless. Thus, this architecture can be used to provide specified input impedance without degrading the noise performance of the amplifier. In order to get  $50 \Omega$  input impedance, set the real part  $(g_{m1}/C_{gs}) L_s$  equal to  $R_s = 50 \Omega$  and the imaginary part  $\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}$  equal to zero at the frequency of interest  $\omega_0$ , which can be obtained through the following expression  $\omega_0 = 1/\sqrt{(L_g + L_s) C_{gs}}$ . In other words, when  $L_g$  and  $L_s$  are in resonant with  $C_{gs}$ , the input impedance  $Z_{in}$  can be made to be equal to  $R_s$ , thus the input matching is achieved. This architecture incorporates  $L_s$  and  $L_g$  to create conjugate matching at the input. The noise factor can be express as

$$F = 1 + \frac{\omega_0}{\omega_T} R_s \gamma g_{d0} + \left[ \frac{\omega_T^2}{\omega_0^2 g_m^2 R_s^2} + 1 \right] R_s \delta g_g + 0.79 R_s \frac{\omega_0}{\omega_T} \sqrt{\gamma g_{d0} \delta g_g} \quad (5.14)$$



**Figure 5.4:** Resistive shunt feedback LNA with active load.

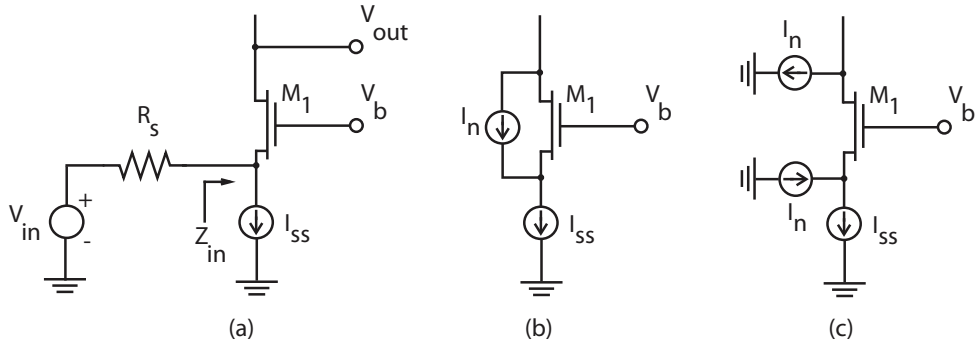
where  $\omega_T \approx g_m/C_{gs}$  is the unity current gain frequency and  $\omega_0$  is the operating frequency. In practice, the gate inductor and source inductor are not ideal. Both have parasitic resistance which will contribute thermal noise. Thus, their effects must be taken into account while doing noise optimization and calculation of input impedance, especially in the case where low-Q on-chip integrated inductors are used. The L-CSLNA is the dominating topology for narrowband systems due to its advantages such as low NF, ease of input matching, high gain and low power consumption. However, these benefits come at the cost of large chip area due to the two inductors; one at the gate and another one at the source of the input device. For those inductors to resonate at low operating frequencies, impractically large inductance values may be required.

### Complementary LNA

When PMOS current source of the RFLNA is converted to an "active load" amplifying the input signal, it forms another wideband topology called complementary LNA as shown in Fig. 5.4. The key idea is that the bias current is reused to provide a higher equivalent transconductance  $g_{m1} + g_{m2}$ .  $M_2$  amplifies the input in addition to injecting noise to the output, then the noise figure may be lower. However, the circuit exhibits a relatively high input resistance. The noise factor is given by

$$F = 1 + \frac{4R_S}{R_F} + \gamma \quad (5.15)$$

The use of complementary or known as current reuse method has been demonstrated in CMOS LNA design to achieve broadband input matching where the equivalent  $50 \Omega$  input impedance is made possible by the couple gate-drain inductors and the loading capacitor [100]. With no additional resistive drain bias circuit in the complementary topology, not only the signal loss can be minimized but also noise performance of the amplifier can also be improved. However, since the two coupled inductors are themselves large and lossy, the unavoidable signal attenuation



**Figure 5.5:** (a) Common gate stage, (b) Inclusion of channel noise, (c) equivalent circuit of (b).

will raise the amplifier's NF. In [101], the UWB LNA mainly utilizes shunt-shunt resistive feedback resistor to achieve input matching. However, the use of the feedback resistor inevitably deteriorates the amplifier's noise. The LNA proposed in [102] combines the complementary topology with asymmetrical inductive source degeneration. By omitting the use of large inductors and a feedback resistor, better noise performance can be expected.

### Common Gate LNA

A wideband LNA topology that has been widely investigated is the common gate low noise amplifier (CGLNA) as shown in Fig. 5.5. The CGLNA is attractive compared to other topologies as it features wideband input impedance matching. This configuration requires that  $1/(g_m + g_{mb}) \approx 1/g_m$  to be equal to  $R_s$ , where  $R_s$  is the  $50\ \Omega$  source resistance. This structure is suitable for wideband input matching designs as  $g_m$  is basically constant over a quite wide frequency range. Therefore, the CGLNA can easily be adopted for broadband impedance matching without many extra components, dramatically saving area and avoiding on-chip inductor resistive losses. Besides, the simple and robust input matching architecture, the CGLNA also has better linearity, lower power consumption and better input-output isolation [103]. The main drawback of this method is that the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise figure. This is due to the input matching condition which restricts a certain value of transconductance to be used that leads to low gain and hence high NF. The NF of the L-CSLNA is generally superior to that of the CGLNA when the operating frequency ( $w_0$ ) is considerably lower than the unit gain frequency ( $w_T$ ) ( $w_0/w_T < 0.2$ ) since CGLNA's NF is limited by  $1/g_m$  input matching. However, the CGLNA provides better noise performance for higher operating frequency ratios  $w_0/w_T$ , as its induced gate noise is only a weak function of  $w_0/w_T$  while the L-CSLNA's noise is proportional to  $w_0/w_T$  [104] [105]. Besides, noise cancellation techniques can be applied to overcome the disadvantage of the CGLNA configuration. The input of a CGLNA and RFLNA form a parallel RLC network, whereas that of a L-CSLNA forms a series network. Again for simplicity of calculation, only the channel

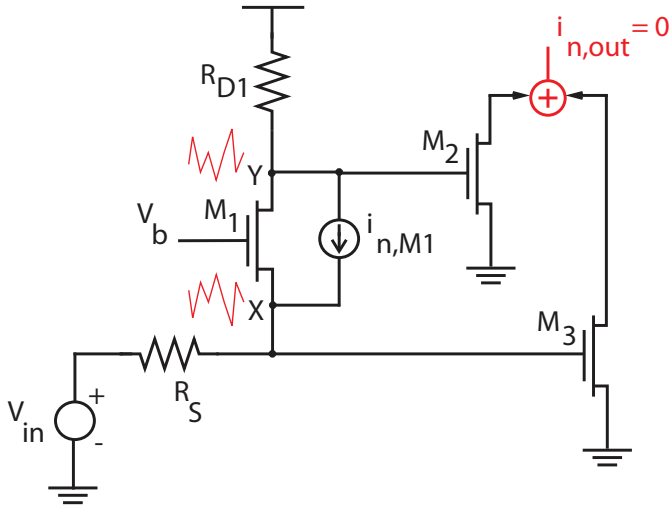


Figure 5.6: CGLNA with noise cancellation.

thermal noise of the MOSFET is taken into account. The noise factor can be expressed as

$$F = \frac{4kTR_S\Delta f \cdot g_m^2 R_D^2 + \overline{i_{nd}^2} R_D^2}{4kTR_S\Delta f \cdot g_m^2 R_D^2} \approx 1 + \frac{\gamma}{\alpha g_m R_S} \quad (5.16)$$

where  $R_D$  is the load resistance at the drain of  $M_1$ . The above equation suggests a reasonable noise figure. However, other noise sources such as gate induced noise and substrate noise can degrade the performance substantially. In short-channel devices,  $\gamma$  can be higher than  $2/3$  while  $\alpha$  can be much less than 1.

### Noise-Cancelling LNA

The purpose of noise cancellation is to generate the noise with the opposite phase-polarities in different paths and cancel the output noise from the matching device. Since the cancellation is irrelevant to the input impedance, this technique allows for simultaneously noise cancellation and impedance matching. The key idea is using an additional auxiliary amplifier which senses the signal and noise voltage then combining the outputs of the main and the auxiliary amplifier such that noise from the input device is cancelled while signal contributions are added at the output node [94]. This section investigates the feedforward noise cancellation technique applied for two specific topologies of CGLNA and RFLNA.

#### CGLNA with Noise Cancellation

Fig. 5.6 illustrates an example of feedforward noise cancellation technique used for a CGLNA. The input matching is accomplished by setting  $1/g_{m1}$  to  $50 \Omega$ . The noise current of  $M_1$  which is modeled by the current source  $I_{n,M1}$ , flows into node X but out of node Y. This creates two fully

correlated noise voltage at nodes X and Y with opposite phases. On the other hand, the signal voltages at nodes X and Y are in phase. The noise voltages at nodes X and Y are converted to currents by  $M_3$  and  $M_2$  respectively. By properly designing  $g_{m2}$  and  $g_{m3}$ , the noise contributed by  $M_1$  can be cancelled at the output. The condition for complete noise cancellation is derived as [107]

$$I_{n,out} = \frac{I_{n,M1}}{1 + g_{m1}R_S} R_{D1}g_{m2} - \frac{I_{n,M1}}{1 + g_{m1}R_S} R_Sg_{m3} = 0 \quad (5.17)$$

$$\Rightarrow g_{m2}R_{D1} = g_{m3}R_S \quad (5.18)$$

where the equivalent transconductance,  $G_m$  is found to be

$$G(m) = \frac{I_{signal}}{V_{signal}} = \frac{1/g_{m1}}{R_S + 1/g_{m1}} (g_{m1}R_{D1}g_{m2} + g_{m3}) \quad (5.19)$$

Compared to resistive shunt feedback amplifiers, the noise factor contributed by the matching device is now fully decoupled with the input matching condition.  $M_2$  can be replaced with a PMOS transistor to reuse the bias current of  $M_3$  if the resultant bandwidth is acceptable. Furthermore, any small signal modeled by a current source and flows between the drain and source of the matching device is cancelled as well (e.g.,  $1/f$  noise, thermal noise of the distributed gate resistance and the bias noise current injected into node Y) [76].

By applying the noise-cancelling technique, the NF is now dominated by  $R_{D1}$ ,  $M_2$  and  $M_3$ . When the input matching condition  $R_S = 1/g_{m1}$  is satisfied, the noise factor contributed by  $R_{D1}$ ,  $M_2$  and  $M_3$  can be derived as

$$F_{RD1} = \frac{4kTR_{D1}g_{m2}^2}{kTR_S(g_{m3} + g_{m2}R_{D1}/R_S)^2} = \frac{R_S}{R_{D1}} \quad (5.20)$$

$$F_{M2} = \frac{4kTg_{m2}\gamma/\alpha}{kTR_S(g_{m3} + g_{m2}R_{D1}/R_S)^2} = \frac{R_S}{R_{D1}} \frac{\gamma}{\alpha} \frac{1}{g_{m2}R_{D1}} \quad (5.21)$$

$$F_{M3} = \frac{4kTg_{m3}\gamma/\alpha}{kTR_S(g_{m3} + g_{m2}R_{D1}/R_S)^2} = \frac{\gamma}{\alpha} \frac{1}{g_{m3}R_S} \quad (5.22)$$

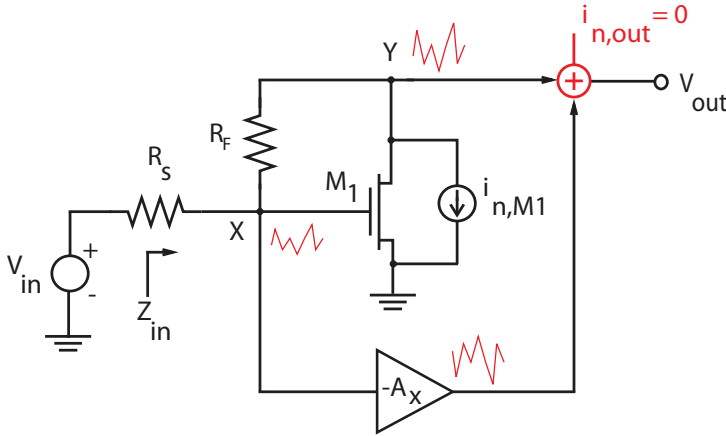
Thus, the total noise factor  $F$  is approximated as

$$F = \frac{R_S}{R_{D1}} + \frac{R_S}{R_{D1}} \frac{\gamma}{\alpha} \frac{1}{g_{m2}R_{D1}} + \frac{\gamma}{\alpha} \frac{1}{g_{m3}R_S} \quad (5.23)$$

### RFLNA with Noise Cancellation

Fig. 5.7 shows a simplified resistive shunt feedback LNA by using the feedforward noise cancellation technique. This LNA is composed of a transistor  $M_1$ , a resistor  $R_F$  and a feedforward voltage amplifier with a gain  $-A_X$ . To have a maximal power transfer, the input impedance  $Z_{in}$  is designed to match to the source impedance,  $R_S$ . Neglecting the loading effect at node Y,  $Z_{in}$  is approximated to  $1/g_{m1}$ , where  $g_{m1}$  is the transconductance of the input transistor  $M_1$ . Again the noise current of  $M_1$  is modeled by the current source  $I_{n,M1}$  between the drain and the source.





**Figure 5.7:** RFLNA with noise cancellation.

The noise current  $I_{n,M1}$  generates the noise voltage  $V_{n,X}$  and  $V_{n,Y}$  at nodes X and Y with the same phase polarity. In contrast, the signal voltages,  $V_X$  and  $V_Y$ , have the opposite-phase polarities, resulting in constructive addition at the output. This is done by creating a new output, where the voltage at node Y is added to a scaled negative replica of the voltage at node X. A proper value for this scaling factor renders noise cancelling at the output node for the thermal noise originating from the matching device [76]. The output noise voltage,  $V_{n,out}$  is given as

$$V_{n,out} = I_{n,M1} (R_S + R_F - A_X R_S) \quad (5.24)$$

To have a zero  $V_{n,out}$ , the gain of the feedforward voltage amplifier should be

$$A_X = 1 + \frac{R_F}{R_S} \quad (5.25)$$

It shows that when  $A_X$  equals to  $1 + (R_F/R_S)$ , the noise of the input transistor  $M_1$  is cancelled at the output. For the signal voltage, the overall voltage gain  $A_V$  can be calculated when  $V_{n,out}$  is cancelled

$$A_V = \frac{V_{out}}{V_X} = (1 - g_{m1} R_F) - A_X = -R_F \left( g_{m1} + \frac{1}{R_S} \right)$$

The cancellation is independent of the input matching condition. For simultaneous input matching and noise cancellation,  $A_V$  equals to  $-2(R_F/R_S)$ . From (5.25) and (5.26),  $A_V$  is increased with  $A_X$  while  $A_X$  is in proportional to  $R_F$ . However, a large  $R_F$  induces noise and degrades the bandwidth. Although the noise of  $R_F$  will be divided by  $A_X$ , the reduction of bandwidth is unavoidable. Therefore, there exists a trade-off between gain and bandwidth, even if the input matching and noise cancellation are both completed [108].

The noise factor at cancellation can be written as [76]

$$F = 1 + \frac{R_S}{R_F} + \frac{\gamma g_{d0}}{g_{m1}^2} \left( \frac{1}{R_S} + \frac{3}{R_F} + \frac{2R_S}{R_F^2} \right) \quad (5.26)$$

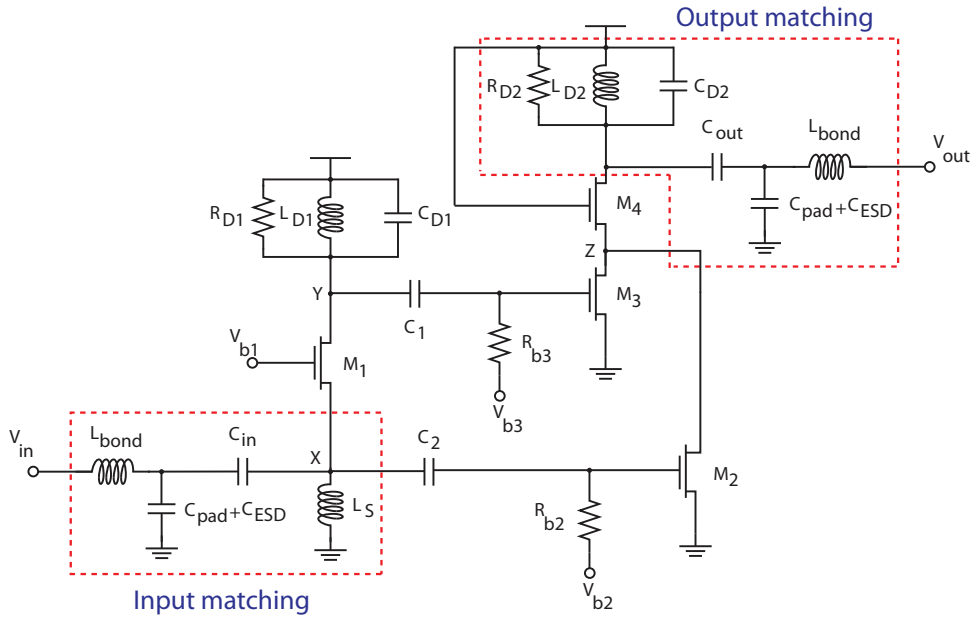


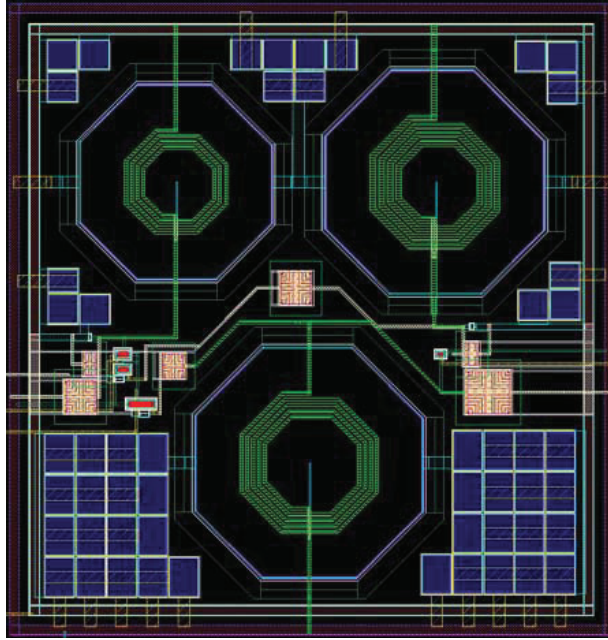
Figure 5.8: The proposed LNA.

### 5.1.4 Proposed 3–5 GHz LNA

Fig. 5.8 shows the schematic of the proposed LNA [Paper II]. It consists of a CG input stage followed by two parallel CS stages that perform noise cancellation. The goal is to adopt the advantages of both CGLNA and noise cancellation technique. The CG topology is chosen for input matching due to the following reasons. First, the CG stage with low input impedance characteristic and broadband behaviour provides NF that is almost independent of the frequency of operation. Besides, the CG stage also eliminates the Miller effect, hence, provides better isolation of the output return signal. However, a single-stage CG amplifier may not have sufficient gain, therefore, a cascade of CG amplifier and cascode CS amplifier has been used to increase the gain. The parasitic inductance of bond wire,  $L_{\text{bond}}$  and parasitic capacitances,  $C_{\text{pad}}$ ,  $C_{\text{ESD}}$  of the bond pad and the ESD protection, respectively, have been taken into account in the design of the proposed LNA. Usually, 1 mm bond wire provides 1 nH inductance. Absorbing parasitic capacitances is relatively simple and is less effected by process variations in the case of the CG topology. The LNA is intended for IR-UWB systems, thus the input matching network needs to have a flat group delay across the passband to keep the distortion of the pulse shape at minimum. The shunt branch inductor,  $L_s$  facilitates the DC biasing by sinking the common drain current of  $M_1$  to the circuit ground.

The size of  $M_3$  is designed for the output bandwidth of the first stage. The LNA can be stabilized by maximizing their reverse isolation, thus adding the cascode transistor  $M_4$  further improves input-output reverse isolation and stability. It also increases the low frequency gain and reduces the input capacitance of the second stage by decreasing the Miller effect due to  $M_3$ .  $C_1$ ,  $C_2$ ,  $C_{\text{in}}$  and  $C_{\text{out}}$  block the DC offset while  $R_{b2}$  and  $R_{b3}$  establish proper biases. Two parallel RLC





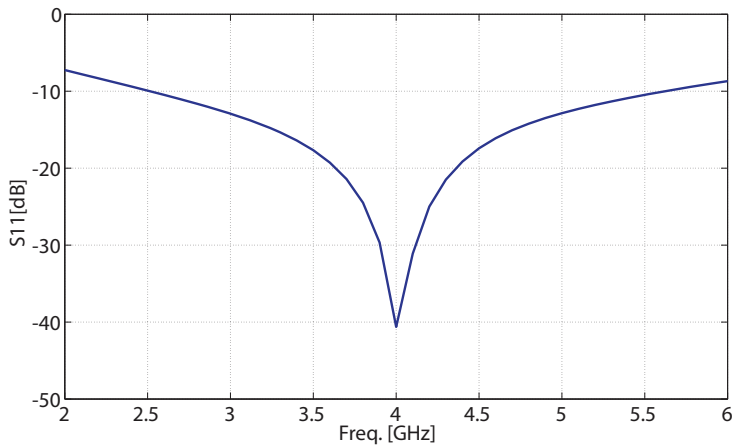
**Figure 5.10:** The LNA layout:  $0.66 \times 0.63 \text{ mm}^2$ .

the proposed LNA.  $S_{11}$  is less than -12 dB while  $S_{22}$  is less than -10 dB over a -3 dB bandwidth of 3–5 GHz. The LNA achieves a peak gain of 17 dB at 4.2 GHz while the reverse isolation is lower than -48 dB, as illustrated in Fig. 5.13 and Fig. 5.14, respectively. A high reverse isolation guarantees high stability for the LNA.

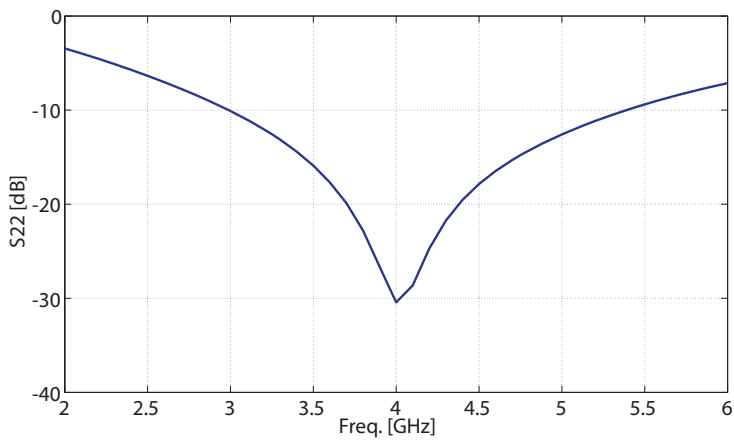
Fig. 5.15 indicates a minimum NF of 2.5 dB and variation of 1 dB across the band of interest. Post-layout simulation results show that noise cancellation effectively lowers the NF over the desired UWB band. Specifically, by applying noise cancellation technique, the NF is reduced by 1.5 dB across the entire band. The linearity of the LNA was estimated. To simulate the input third-order intercept point (IIP3), a two-tone signal separated by 50 MHz was used. Fig. 5.16 shows the fundamental frequency and two-tone third-order intermodulation output powers at input RF frequency of 4 GHz. The input referred 1 dB compression point (P1dB) is -18 dBm while the IIP3 is -8 dBm. The LNA consumes 12.5 mW from a 1.2 V supply voltage. Table 5.1 summarizes the performance of the proposed LNA and compares it to other published designs operating in a similar frequency range.

### 5.1.6 Summary

A 3–5 GHz LNA has been demonstrated in 90 nm CMOS technology [Paper II]. The input CG stage has been exploited together with noise-cancelling technique to obtain broadband input matching and noise cancellation simultaneously. Resonant RLC loads with second order band-pass characteristics reject out-of-band interferers while offer high gain. The proposed LNA occupies an area of only  $0.4 \text{ mm}^2$ , which facilitates a low cost design. Post-layout simulation



**Figure 5.11:** The simulated input return loss,  $S_{11}$  versus frequency.



**Figure 5.12:** The simulated output return loss,  $S_{22}$  versus frequency.

**Table 5.1:** Comparison with the previous published LNAs

Ref.	CMOS tech.	Die area (mm <sup>2</sup> )	Power cons. (mW)	-3 dB BW (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)
[74]	65 nm	—	20	0.2–5.2	15.6	3.5	0
[95]	0.13 $\mu$ m	0.025	5.7	0.2–3.8	19	2.8–3.4	-4.2
[110]	0.18 $\mu$ m	0.9	12.6	2–4.6	9.8	2.3–5.2	-7
[111]	90 nm	0.2	8	2.5–4	19.6	4	-8
[112]	90 nm	—	12.5	0.8–6	18–20	3–3.5	-3.5
[113]	90 nm	0.002	9.8	0–6	17.4*	2.5	-10
This work	90 nm	0.4	12.5	3–5	17	2.5–3.5	-8

\*power gain

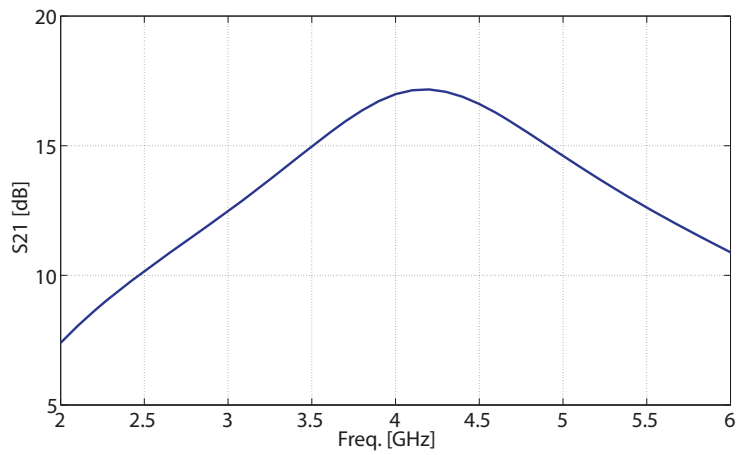


Figure 5.13: The simulated gain,  $S_{21}$  versus frequency.

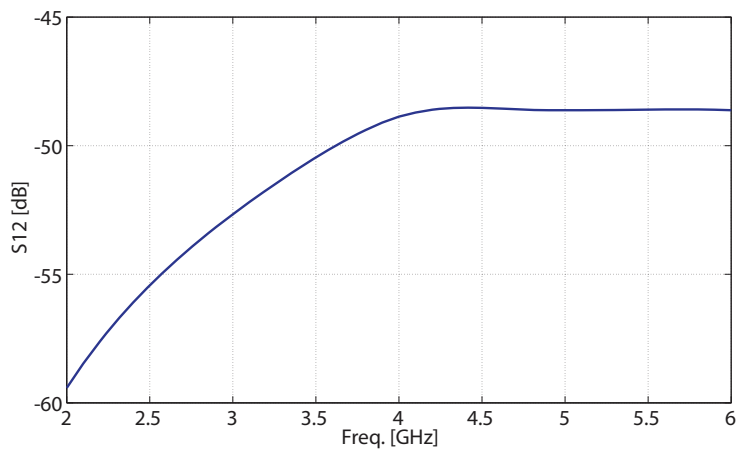


Figure 5.14: The simulated reverse isolation,  $S_{12}$  versus frequency.

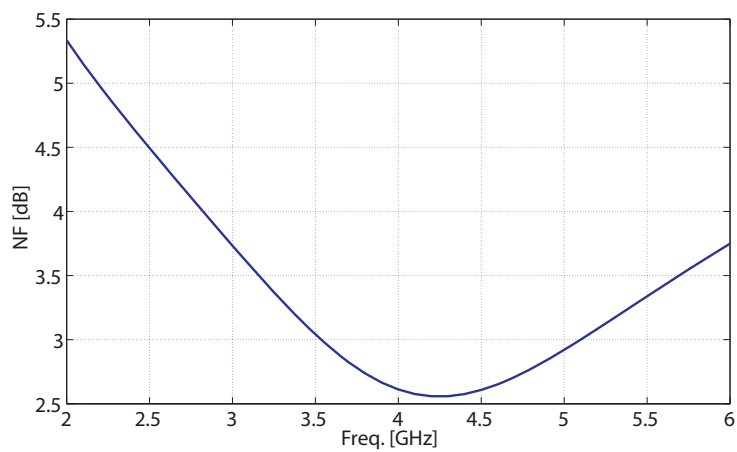


Figure 5.15: The simulated NF versus frequency.

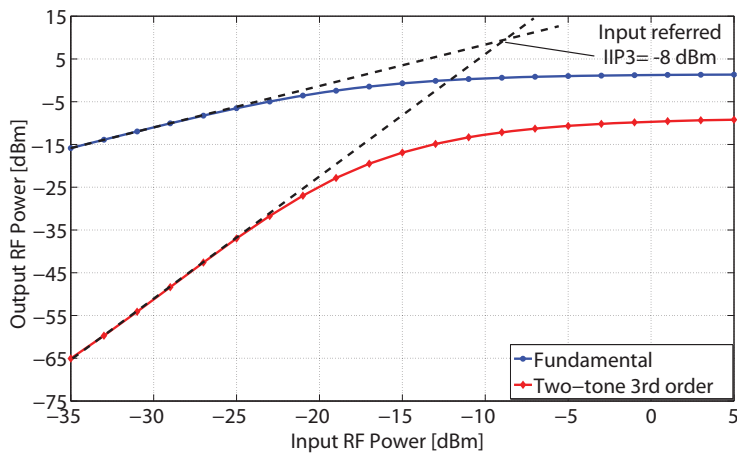


Figure 5.16: The simulated linearity of the LNA at mid-band RF frequency of 4 GHz.

results show a peak gain of 17 dB, a NF of 2.5–3.5 dB over the entire -3 dB bandwidth from 3 GHz to 5 GHz and an IIP3 of -8 dBm while consuming 12.5 mW from a 1.2 V supply voltage.

## 5.2 Mixers

### 5.2.1 Introduction

The mixers in the transmitter and the receiver perform the frequency up and down conversions, respectively by multiplying the incoming signal either in the baseband or the intermediate frequency (IF) band or the radio frequency (RF) band with the signal from the local oscillator (LO). The IF/RF port senses the signal to be converted while the LO port senses the periodic waveform generated by the local oscillator. Ideally, the mixer shifts the input frequency to another frequency according to equation

$$f_{\text{out}} = \pm f_{\text{LO}} \pm f_{\text{in}} \quad (5.28)$$

In practice, due to the non-linearity of the device or large signals used in the mixers, there are also intermodulation products determined by

$$f_{\text{out}} = m f_{\text{LO}} + n f_{\text{in}} \quad (5.29)$$

where  $m$  and  $n$  are  $\pm$  integers and  $f_{\text{in}}$  is the center frequency of the incoming signal.

### 5.2.2 Performance Parameters

#### Conversion Gain

The conversion gain of a downconversion mixer is given by the ratio of the RMS voltage of the IF signal to the RMS voltage of the RF signal in which these two signals are centered around two different frequencies. The voltage conversion gain can be measured by applying a sinusoid at  $w_{\text{RF}}$  and finding the amplitude of the downconverted component at  $w_{\text{IF}}$ . For upconversion mixers, the voltage conversion gain is defined in a similar way but from the baseband or IF port to the RF port.

#### Noise Figure

The noise figure is defined as the SNR at the input port divided by the SNR at the output port. In general, if the desired signal exists at only one frequency and there is no desired signal at the image frequency then the measured NF is called single-sideband (SSB) NF. In rarer case, where both the desired signal and the image signal contain useful information, leads to a double-sideband (DSB) NF. The SSB NF will normally be 3 dB higher than the DSB NF.



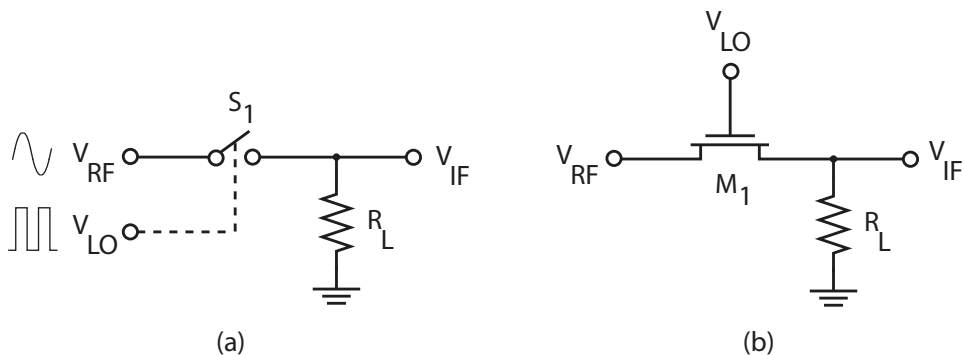


Figure 5.17: A passive mixer.

### Linearity

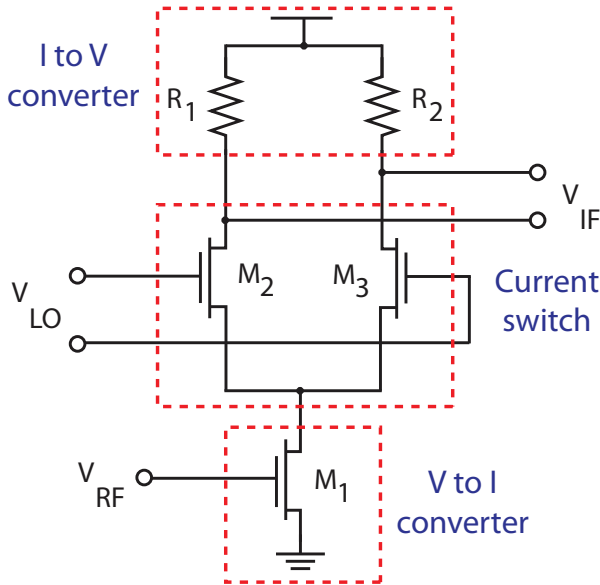
The linearity of the mixer is expressed in term of 1 dB compression point (P1dB) or third order intercept point (IP3). The 1 dB compression point is the value at which the RF output signal deviates from linear operation by 1 dB. At this point the output power no longer increases in direct proportion to the input power but begins to level off. A further test of the non-linearity is the intercept point. This is a measure of the generation of intermodulation products at  $2\omega_2 - \omega_1$  and  $2\omega_1 - \omega_2$  when two tones of frequency  $\omega_1$  and  $\omega_2$  are applied at the input. When plotted on a logarithmic scale, the magnitude of the intermodulation products grows at three times the rate of the fundamental frequency and the point of intersection is called the third order intercept point. The horizontal component is referred to as the input IP3 (IIP3) while the vertical component is called the output IP3 (OIP3).

### Port-to-Port Feedthrough

The isolation between each ports of a mixer is critical. The LO-RF feedthrough results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feedthrough is important because if substantial LO signal exists as the IF output even after low-pass filtering, then the following stage may be desensitized. Finally, the RF-IF isolation determines what fraction of the signal in the RF path directly appears in the IF, a critical issue with respect to the even-order distortion problem in homodyne receivers [30].

### 5.2.3 Passive and Active Mixer

The spectrum of the incoming signal can be shifted up or down by  $\pm f_{LO}$  to the desired frequency. This can be seen in the simple circuit of Fig. 5.17a, where the output is equal to the RF input when  $S_1$  is on and zero when  $S_1$  is off. This operation can also be viewed as multiplication of the RF signal by a waveform. The circuit is a linear, time-variant system with respect to the RF port and a nonlinear, time-variant system with respect to the LO port. Normally, the signal



**Figure 5.18:** An active mixer.

amplified by the LNA (and possibly filtered by an image-reject filter) is applied to the RF port of the mixer. Thus, this port must exhibit sufficiently low noise and high linearity, the latter because nearby interferers are amplified by the LNA and hence can produce stronger intermodulation products. If the circuit of Fig. 5.17a incorporates a MOS switch as shown in Fig. 5.17b then the on-resistance of the transistor contributes noise. Furthermore, as the RF input signal varies, the gate-source overdrive voltage of  $M_1$  and hence its on-resistance change, introducing nonlinearity in the voltage division between  $M_1$  and  $R_L$ .

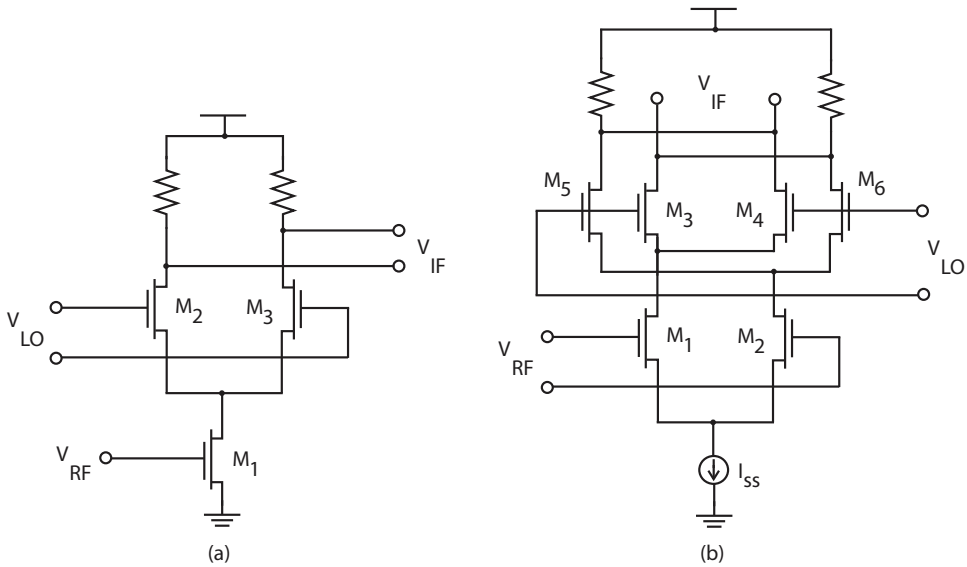
The circuit of Fig. 5.17b is an example of passive mixers because it does not provide any gain. By contract, active mixers generally provide gain. Shown in Fig. 5.18, is an example, where the RF input varies the drain current of  $M_1$  while  $M_2$  and  $M_3$  function as a switching pair driven by the LO. Thus, the drain current of  $M_1$  is in essence multiplied by a square wave as it is routed to  $R_1$  and  $R_2$  alternately. For  $R_1 = R_2 = R_D$ , the voltage conversion gain is equal to

$$A_V = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_{m1} R_D \quad (5.30)$$

The input-referred noise voltage is given by

$$\overline{V_{n,in}^2} = \pi^2 kT \left( \frac{\gamma}{g_{m1}} + \frac{2}{g_{m1}^2 R_D} \right) \quad (5.31)$$

If a mixer accommodates a differential LO signal but single-ended RF signal, it is called "single-balanced" as shown in Fig. 5.19a. If a mixer operates with both differential LO and RF inputs, then it called "double-balanced", the active version of which is well known as Gilbert cell as shown in Fig. 5.19b. The single-balanced configuration exhibits less input-referred noise



**Figure 5.19:** (a) Single-balanced active mixer and (b) Double-balanced active mixer.

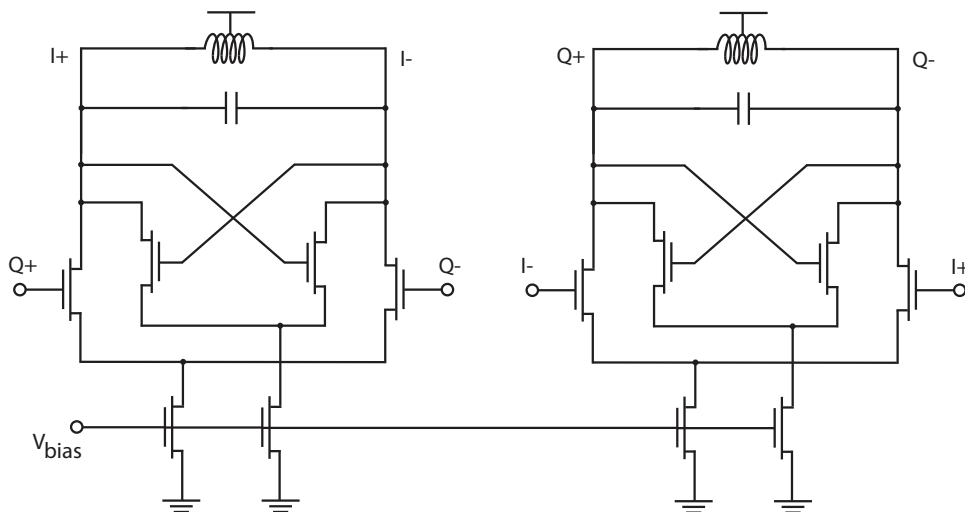
for a given power dissipation than the double-balanced counterpart. However, the circuit is more susceptible to noise in the LO signal. The double-balanced mixer generates less even-order distortion, thus relaxing the half-IF issues in heterodyne receivers and lowering the beat components in homodyne architectures. Nevertheless, since the RF signal processed by the LNA is usually single-ended, one of the input terminals of the double-balanced mixer is simply connected to a bias voltage. This in turn creates different propagation times or phase shifts for the two signal phases amplified by  $M_1$  and  $M_2$  leading to finite even-order distortion.

By virtue of their gains, active mixers reduce the noise contributed by subsequent stages and are widely used in RF systems. Passive mixers, on the other hand, typically achieve a higher linearity and speed and find applications in microwave and base station circuits.

### 5.2.4 Proposed Downconversion Quadrature Mixer

The RF signals amplified by the LNA are then downconverted to baseband by a mixer. Down-conversion of any asymmetrically-modulated signal to a zero IF lead to cancellation unless the baseband signals are separated by their phases, thus a quadrature mixer is necessary. In addition, linearity requirement has a large impact on the choice of mixer topologies. When linearity considerations are insignificant, Gilbert Cell mixers can be employed instead of other topologies for superior noise and gain characteristics. The quadrature mixer is proposed in Fig. 5.20 [Paper II]. It is a wideband modified Gilbert Cell mixer. A single common-source transconductor ( $M_1$ ) injects the RF signal in two single-balanced quadrature commutative pairs. Compared to double-balanced Gilbert Cell based mixer adopting two separate transconductors, this proposed mixer allows a higher switching pair current gain [114]. In addition, the parasitic capacitance loading the previous stage is minimized for the same transconductance gain. The





**Figure 5.21:** The conventional QVCO.

modes randomly or the VCO may jump between these two modes during operation. While the problem appears to be an inherent drawback of the QVCO topology, various options to prevent bimodal oscillation from happening in a real circuit were explored. Li et al. [120] swept an artificial phase shift introduced into the coupling path over a complete clock (from  $0^\circ$  to  $360^\circ$ ) of the oscillation frequency. It can be found that the QVCO will stay in a stable oscillation mode until the phase shift reaches a certain value at which the QVCO will become unstable again. Increasing the phase shift further will pull the VCO out of the unstable bimodal state and the QVCO will stably oscillate in another mode. Over the  $360^\circ$  phase range, four unstable boundaries will be encountered. Every time an unstable boundary is crossed, the oscillation mode will switch from one mode to the next.

One important observation is that if a certain amount of phase shift is introduced into the coupling path to deviate from the boundaries, the QVCO will not experience any bimode oscillation even though the RLC components of LC-tanks or the bias currents of the VCO cores are perturbed over a relatively large range. In [121], a resistor is added at the gate of each coupling transistor to realize an RC low-pass network with the gate capacitance. However, the phase noise performance would be degraded because of the extra noise added by resistor. In [120], it is suggested to replace the regular differential coupling pair with cascode topology. The cascode creates a phase delay which moves the QVCO operation away from the unstable boundary, thus giving QVCO adequate phase margin to ensure the VCO stays in a stable mode, ultimately eliminating bimodal oscillation.

### Proposed QVCO

The proposed QVCO is shown in Fig. 5.22 [Paper II]. The complementary cross-coupled LC oscillator has been exploited in this design. By reusing the current of NMOS transistor for PMOS

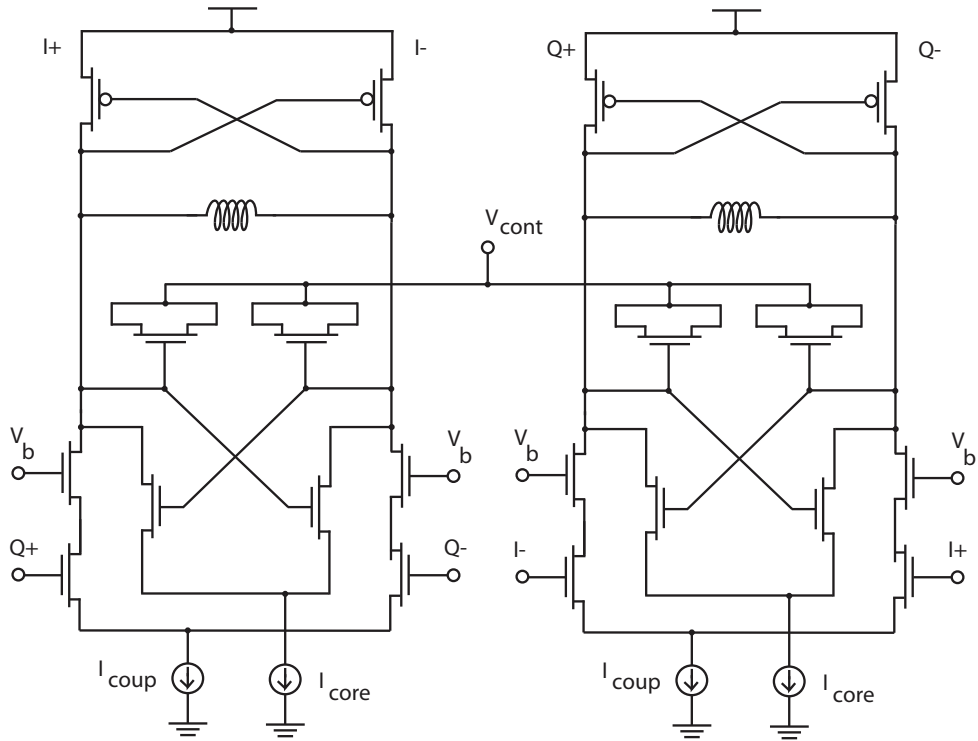


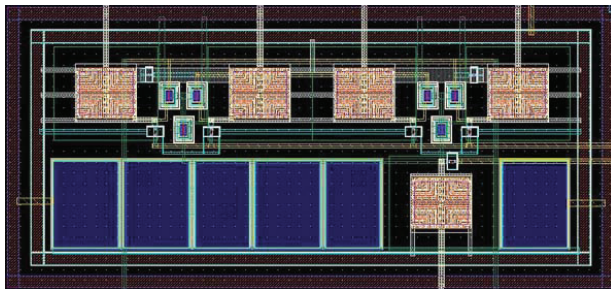
Figure 5.22: The proposed QVCO.

transistor, the total transconductance is  $g_{mn} + g_{mp}$  compared to just  $g_{mn}$  of a non-complementary VCO with the same current. Where  $g_{mn}$  and  $g_{mp}$  are the transconductance of NMOS transistor and PMOS transistor, respectively. Due to the larger  $g_m$ , the amplitude of oscillation is increased. This results in less phase noise and faster switching for a cross-coupled differential pair. In addition, the complementary VCO is able to have a symmetric LC tank by designing such that  $g_{mn} = g_{mp}$ . Consequently, the flicker noise upconversion is reduced, thus further decreasing the phase noise [98].

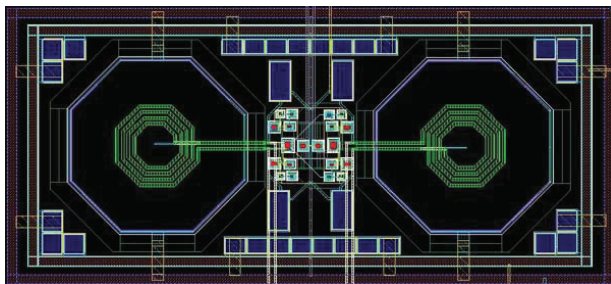
### 5.2.5 Post-Layout Simulation Results

The proposed mixer was designed in 90 nm CMOS to operate between 1 GHz and 6 GHz with an on-chip QVCO. The mixer core occupies an area of  $0.03 \text{ mm}^2$  while the QVCO occupies an area of  $0.2 \text{ mm}^2$  as shown in Fig. 5.23 and Fig. 5.24, respectively. For all simulation results, the IF is always kept at a constant 100 MHz while the RF and LO frequencies are being changed together with the LO being 100 MHz lower than the RF. To simplify the simulation, one of the IF signal is simulated while the other is terminated to a  $50 \Omega$  load resistor.

Post-layout simulation results show that the LO frequency can be varied between 3.4 GHz and 4.6 GHz with respect to varactor control voltage as plotted in Fig. 5.25. The varactors are realized by NMOS transistors. The amplitude imbalance remains within  $\pm 0.3 \text{ dB}$  while the



**Figure 5.23:** The mixer layout:  $0.28 \times 0.12 \text{ mm}^2$ .



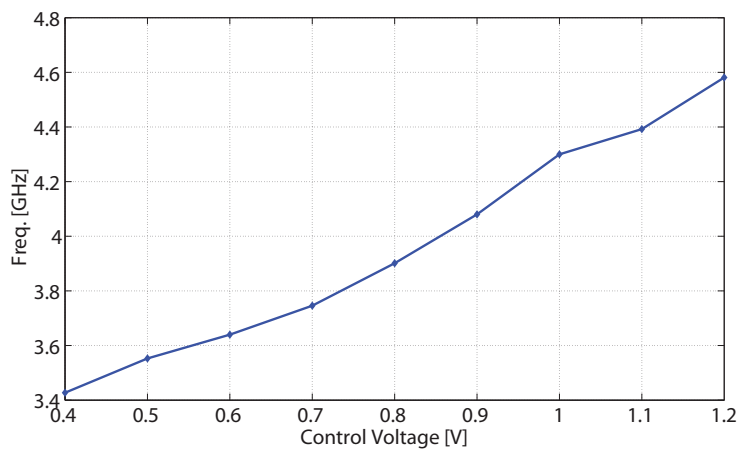
**Figure 5.24:** The QVCO layout:  $0.63 \times 0.29 \text{ mm}^2$ .

quadrature phase error is less than  $\pm 1^\circ$  over the operating frequencies. An example of the quadrature signals generated by the proposed QVCO are plotted in Fig. 5.26. Fig. 5.27 plots the mixer conversion gain as a function of the RF input frequency. It exhibits a peak conversion gain of 9 dB for a fixed LO frequency of 4 GHz. Fig. 5.28 shows the port-to-port isolation. The RF-to-IF and RF-to-LO isolation exceed 40 dB and 50 dB, respectively, while those for LO-to-RF and LO-to-IF are 30 dB over the RF band from 1 GHz to 6 GHz. A second-order RC low-pass filter loads the mixer further suppressing the residual LO signal at the IF port.

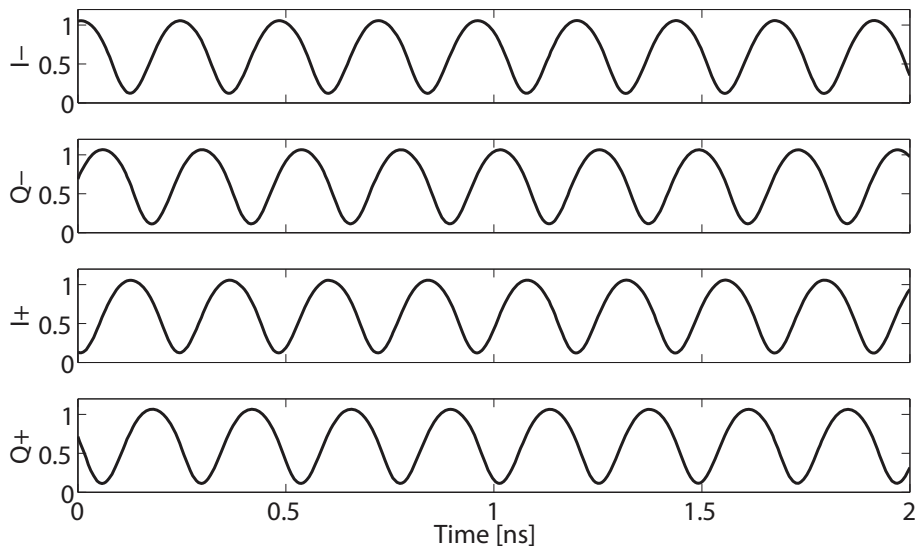
At a mid-band RF frequency of 4 GHz, the simulated third-order intermodulation with a frequency spacing of 50 MHz is plotted in Fig. 5.29. The proposed mixer obtains an IIP3 of 0.5 dBm and P1dB of -8.5 dBm. The NF is also estimated at the fixed output frequency of 100 MHz. The mixer exhibits the NF of 6-8 dB across the entire band. Operating at a 1.2 V supply voltage, the total power consumption of the proposed mixer is 6.2 mW including the QVCO dissipation. In order to evaluate the performance of the proposed mixer, the previously reported CMOS mixers and this work are compared in table 5.2.

### 5.2.6 Summary

A modified Gilbert Cell mixer with two quadrature pairs sharing the same input transconductor was designed using TSMC 90 nm CMOS technology [Paper II]. The single-balanced topology is chosen in this design to avoid a single-to-differential converter required at the input of the mixer and to have less noise compared to double-balanced Gilbert Cell based mixer. Along with the mixer is an on-chip QVCO based on two complementary cross-coupled LC oscillators. The



**Figure 5.25:** The simulated oscillation frequency of the QVCO with respect to varactor control voltage.



**Figure 5.26:** The simulated quadrature LO signals generated by the QVCO.

**Table 5.2:** Comparison with the previous published mixers

Ref.	CMOS tech.	Die area (mm <sup>2</sup> )	Power cons. (mW)	RF freq. (GHz)	CG (dB)	NF (dB)	IIP3 (dBm)
[122]	0.18 μm	0.03	0.28	0.5–6	6	12.2	0
[123]	0.18 μm	0.1	5.4	0.5–3	9.5	16.5	10
[124]	0.13 μm	0.13	16.8	0.9–3.7	14	2.7–6.5	-10
[125]	0.13 μm	0.3	34.5	1–5.5	17.5	3.9	0.8
This work	90 nm	0.23*	6.2*	1–6	8±1	6–8	0.5

\*with QVCO



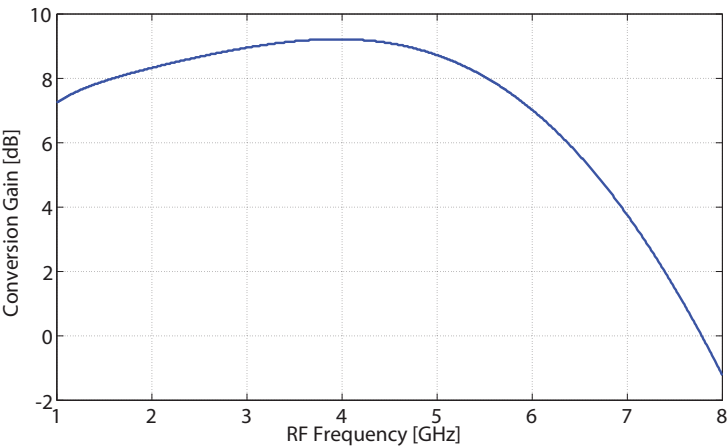


Figure 5.27: The simulated mixer conversion gain.

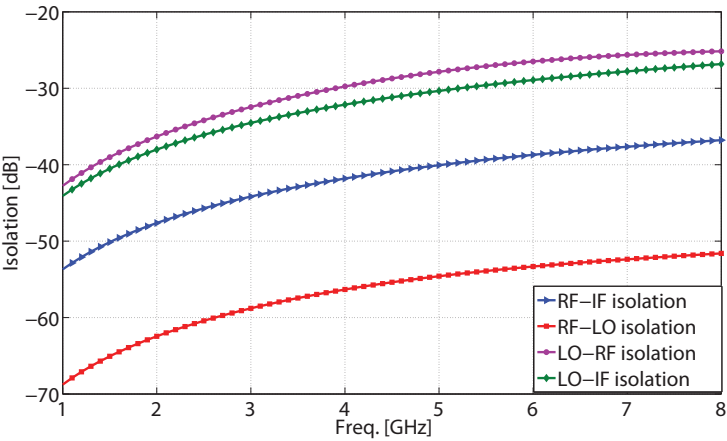
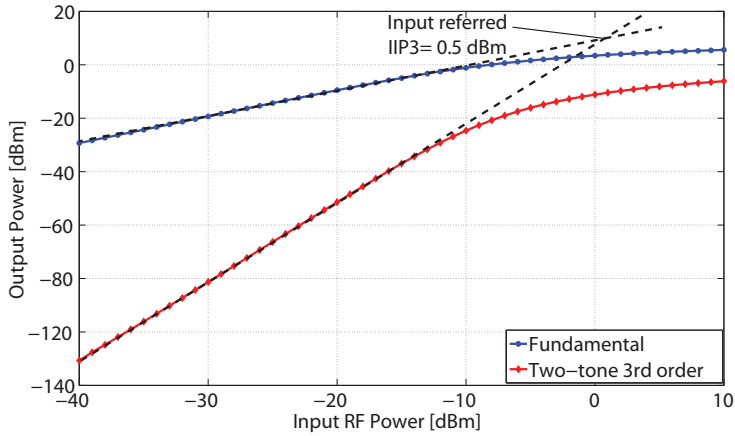


Figure 5.28: The simulated port-to-port isolation.



**Figure 5.29:** The simulated linearity of the mixer at mid-band RF frequency of 4 GHz.

complementary configuration is exploited to increase the amplitude oscillation as well as reduce phase noise. The proposed mixer has good performance in terms of linearity with IIP3 of 0.5 dB at 4 GHz. It obtains the conversion gain of  $8 \pm 1$  dB and noise figure of 6-8 dB over the entire bandwidth from 1 GHz to 6 GHz while consuming 6.2 mW of power with a supply voltage of 1.2 V.

# Chapter 6

## UWB VIVALDI ANTENNAS

### 6.1 Introduction

For UWB radio systems, a lot of antennas have been designed and tested. The design of UWB antennas in CMOS should be avoided due to their big sizes as well as the lossy nature of the CMOS substrate. Requirements for antennas vary with applications and systems. Methods to categorize antennas can be highlighted in terms of their operating frequency, geometry, function, materials, etc. In terms of geometry and radiation characteristics, they may be two or three-dimensional designs and omnidirectional or directional designs [126]. Horn and reflector antennas are typical three-dimensional high-gain directional solutions, which have been studied widely and they are usually employed in test or point-to-point applications. However, its bulky design is not suitable for applications with size constraint such as portable devices. Among two-dimensional directional solutions, Vivaldi antennas are widely used for UWB systems. The Vivaldi antenna is one of the classical UWB antennas which was first investigated by P. Gibson in 1979 and many improvements to the initial design have since been presented [127] [128]. A Vivaldi antenna is basically a planar traveling wave antenna with end-fire radiation. A variety of taper profiles of those slots have been presented, such as exponential, tangential, parabolic, linear-constant, exponential-constant, step-constant and linear profiles. After being invented, the Vivaldi antenna is the preferred candidate for UWB applications due to its wide bandwidth, low cross polarization and highly directive patterns [129]. There are many advantages of using directional antennas in both UWB impulse radar and communications. First of all, the energy efficiency is good. While a standard omnidirectional antenna transmits the energy in all directions, a directional antenna is capable of directing most emitted power in a lobe or beam. In this way a receiving antenna can get more of the radiated energy, thus reducing the required transmission power. The high directivity is important for focusing most of the radiated energy in well-controlled beams. Moreover, optimal UWB pulse reception entails minimization of ringing, spreading and distortion of the pulse at the transmit and receive antennas. This requires sufficient impedance matching and near constant group delay throughout the entire bandwidth.

In this chapter, two different Vivaldi antennas are designed and tested [**Paper X**]. The first is an antipodal Vivaldi antenna while the other is a tapered slot Vivaldi antenna. They are both designed for the 1 GHz to 5 GHz frequency band with low impulse distortion and the voltage

standing wave ratios (VSWR) are less than 2 throughout the entire bandwidth.

## 6.2 Antenna Parameters

### 6.2.1 Bandwidth

The antenna frequency bandwidth is the frequency range it operates satisfactory.

$$BW = f_U - f_L \quad (6.1)$$

where  $f_U$  is the upper operational frequency limit and  $f_L$  is the lower operational frequency limit.

### 6.2.2 VSWR

Voltage standing wave ratio is a function of the reflection coefficient which describes the power reflected from the antenna.

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (6.2)$$

where  $\Gamma$  is the reflection coefficient, defined as

$$|\Gamma| = \left| \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \right| \quad (6.3)$$

### 6.2.3 Radiation Efficiency

The efficiency of an antenna is the ratio between the power radiated or dissipated by the antenna,  $P_{rad}$  and the power delivered to the antenna,  $P_t$ .

$$\eta = \frac{P_{rad}}{P_t} \quad (6.4)$$

where  $P_{rad}$  is calculated as followed

$$P_{rad} = \int_0^{2\pi} \int_0^\pi S_t(\theta, \phi) r^2 \sin\theta d\theta d\phi \quad (6.5)$$

where  $S_t(\theta, \phi)$  is the power density (in  $W/m^2$ ) and the average power density being

$$P_{avg} = \frac{P_{rad}}{4\pi r^2} \quad (6.6)$$

### 6.2.4 Radiation Pattern

A radiation pattern defines the variation of the power radiated by an antenna as a function of the direction away from the antenna. This power variation as a function of the arrival angle is

observed in the antenna's far field. The average radiation intensity  $U$  (watt per unit solid angle) at a given distance  $r$  is

$$U_{\text{avg}} = r^2 P_{\text{avg}} = \frac{P_{\text{rad}}}{4\pi} \quad (6.7)$$

### 6.2.5 Directivity

Directivity is a measure of the antenna to concentrate radiated power in a particular direction and it is related to power density as

$$D_t(\theta, \phi) = \frac{S_t(\theta, \phi)}{P_{\text{avg}}} = \frac{S_t(\theta, \phi)}{P_{\text{rad}}/(4\pi r^2)} \quad (6.8)$$

### 6.2.6 Gain

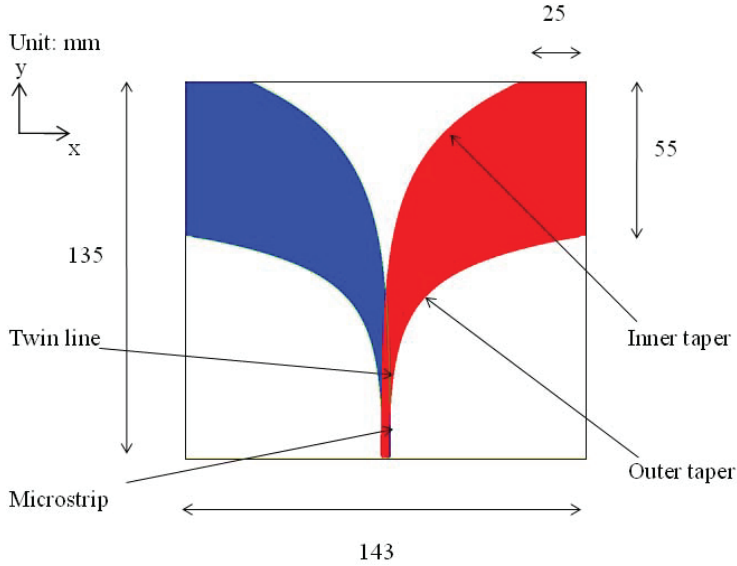
The power gain  $G$  or simply gain is the ratio between the radiation intensity in a direction and the radiation intensity to an isotropic loss free antenna with the same input power. It is related to antenna efficiency and directivity as followed

$$G(\theta, \phi) = \eta D_t(\theta, \phi) \quad (6.9)$$

## 6.3 Vivaldi Antennas

Impulse radio systems are carrier-free, thus distortion of the waveforms of the transmitted pulses may significantly degrade quality of wireless communications by impulse radio systems. These features of the impulse transmission differentiate the design considerations of UWB antennas for impulse radio systems from conventional narrowband and even broadband radio systems. A Vivaldi antenna is formed by elliptically tapering the inner and outer edges of the slotline conductors. Theoretically, Vivaldi antennas have an unlimited range of operating frequencies with constant beamwidth over the entire bandwidth. In addition, a major advantage of this antenna type is that the ultra wide bandwidth can be achieved using antipodal tapered profiles and exponential tapered profiles with its inherently simple wideband transition from microstrip line to parallel-strips [130]. As a result, the distortion in the waveform of radiated pulses by the Vivaldi antenna is small making it a potential candidate for IR-UWB.

Two different Vivaldi antennas were fabricated on Rogers RO4350B substrate with a relative constant of 3.48, thickness of 1.52 mm and loss tangent of 0.0031 [**Paper X**]. These antennas were designed for first derivative Gaussian pulse transmission. The pulses fill a bandwidth from 1 GHz to 5 GHz. To transmit and receive such short-duration Gaussian pulses, the wide bandwidth of the antenna is crucial for reducing distortion. All parameters of the Vivaldi antennas were optimized by Ansoft High Frequency Structure Simulator (HFSS) and then fabricated to perform S-parameter measurements for validation. The measurement results are obtained using ZVB 20 Vector Network Analyzer. Both antipodal and tapered slot Vivaldi antenna match the feeding port to 50  $\Omega$ . They all have small dimensions and good performance.



**Figure 6.1:** Structure and designed parameters of antipodal Vivaldi antenna.

### 6.3.1 Antipodal Vivaldi Antenna

The structure and designed parameters of the antipodal Vivaldi antenna are depicted in Fig. 6.1. It comprises tapered radiating slot and feeding transition. A smooth transition between twin line and microstrip line is used to remove the bandwidth limitation of transition in the conventional Vivaldi antenna. The microstrip line and ground plane are on different sides of the substrate and gradually flare out in opposite directions to form the tapered slot. The symmetrical pair of conductor serves as an impedance transformer, leading to gradual change of impedance from  $50 \Omega$  in the feed of the antenna to free space in the end. The assigned dimensions are developed for the specified frequency band.

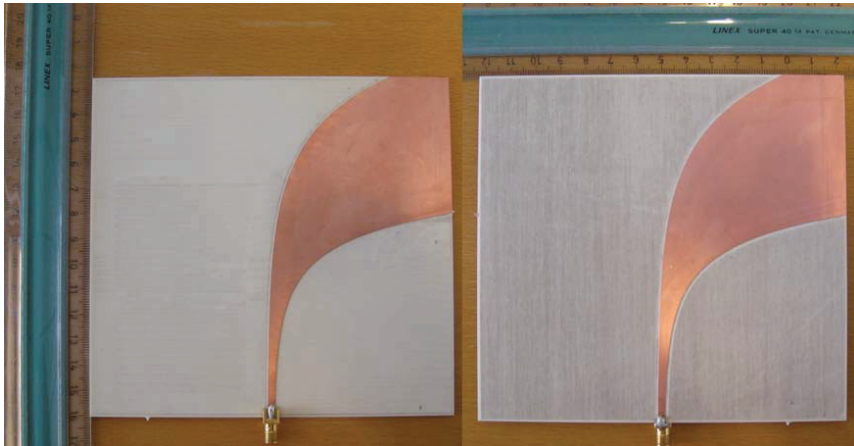
Since the antipodal Vivaldi antenna operate as a resonant antenna at the lower end of frequency band, the antenna width  $W$  is determined based on lower edge operating frequency  $f_{\min}$  and effective dielectric constant  $\epsilon_{\text{eff}}$  in the following equation [131]

$$W = \frac{c}{2 \times f_{\min} \times \sqrt{\epsilon_{\text{eff}}}} \quad (6.10)$$

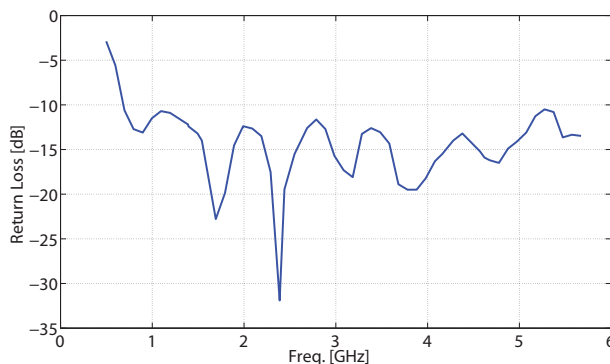
Thus, an increased antenna width affects the lower end in its frequency band.

### Measurement Results

Fig. 6.2 displays the top view and bottom view of the designed antipodal Vivaldi antenna. As depicted in Fig. 6.3 and Fig. 6.4, the antipodal Vivaldi antenna presents good return loss better than -10 dB over the wide bandwidth from 1 GHz to 5 GHz. In most of frequency band, VSWR less than 1.5 indicating that the reflection coefficient is less than 0.2 across the quoted frequency range. Hence, of the power delivered to the antenna, only 4% of the power is reflected back to the



**Figure 6.2:** Top view and bottom view of antipodal Vivaldi antenna.



**Figure 6.3:** Measured return loss of antipodal Vivaldi antenna.

transmitter. Moreover, the ground plane around the feeding port is removed in this antenna. The removal of the ground plane is derived from the investigation in [131]. This leads to an increase of the impedance bandwidth without changing the radiation pattern. Consequently, measurement results of S-parameters ( $S_{11}$ ,  $S_{12}$ ) and VSWR show that the antipodal Vivaldi antenna has a very wide bandwidth and it can be used for applications using frequency bands up to 20 GHz. Fig. 6.5 is the phase behavior of the antenna. It can be seen that the antenna has a good linear phase response.

The antenna gain versus frequency is given in table 6.1 and plotted in Fig. 6.6. The gain is measured at the distance of 1 m. Overall, this antenna has high gain values as in most part of the frequency band, the gain is higher than 6 dBi. For comparison, the small antipodal Vivaldi antenna in [132] has the gain less than 6 dBi. Due to the lack of good facilities and measurement conditions, only simulated radiation pattern of the antipodal Vivaldi antenna is given as shown in Fig. 6.7. At 2 GHz, the half-power beamwidths are  $100^\circ$  in the E-plane/Azimuth and  $80^\circ$  in the H-plane/Elevation. The designed antipodal Vivaldi antenna has a small backward radiation in both E-plane plane and H-plane plane. As a result, its directivity is remarkably improved in

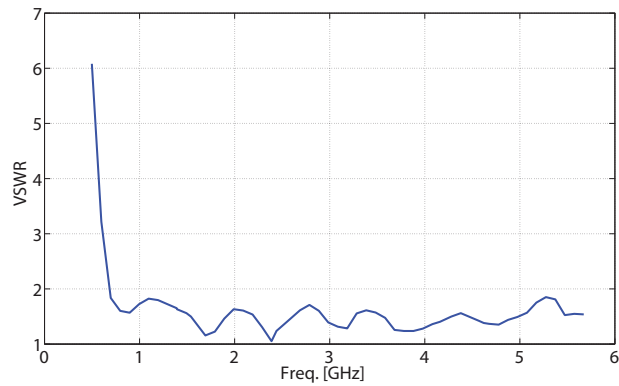


Figure 6.4: Measured VSWR of antipodal Vivaldi antenna.

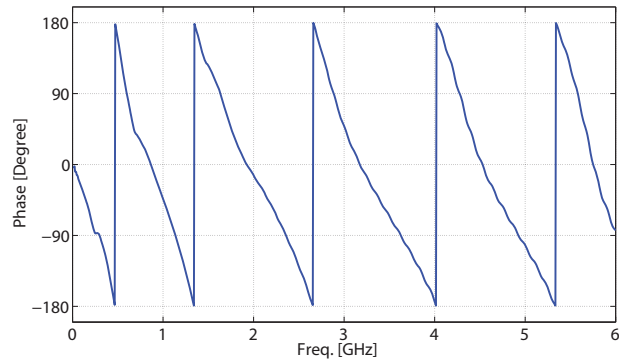
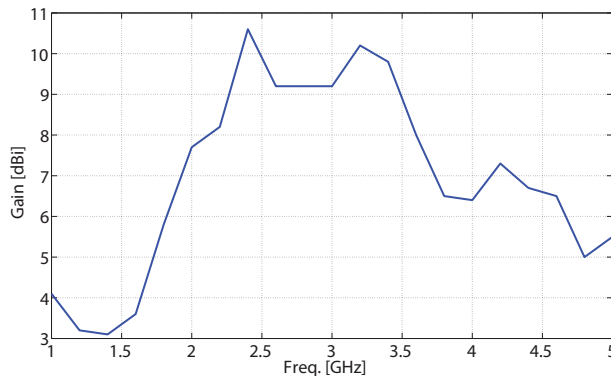


Figure 6.5: Measured phase response of antipodal Vivaldi antenna.

Table 6.1: Measured gain values of antipodal Vivaldi antenna.

Freq (GHz)	Gain (dBi)	Freq (GHz)	Gain (dBi)
1.00	4.10	3.20	10.20
1.20	3.20	3.40	9.80
1.40	3.10	3.60	8.00
1.60	3.60	3.80	6.50
1.80	5.80	4.00	6.40
2.00	7.70	4.20	7.30
2.20	8.20	4.40	6.70
2.40	10.60	4.60	6.50
2.60	9.20	4.80	5.00
2.80	9.20	5.00	5.50
3.00	9.20		





**Figure 6.6:** Measured gain versus frequency of antipodal Vivaldi antenna.

comparison with the antipodal Vivaldi antenna in [131] and in [132].

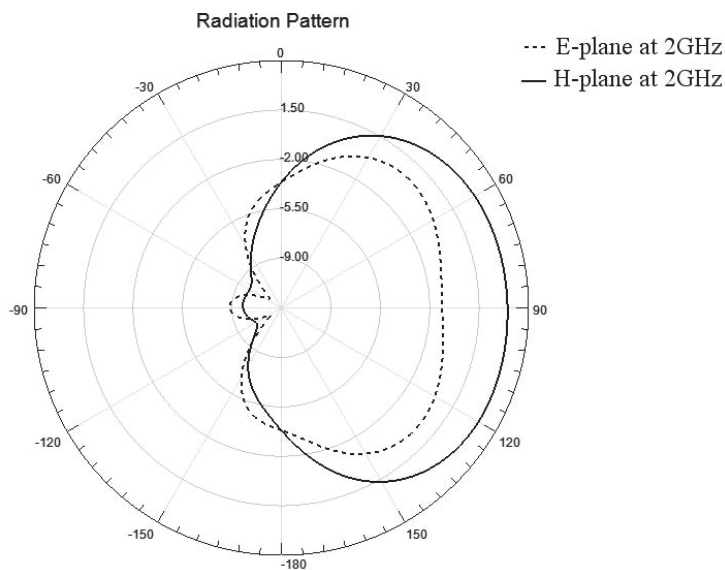
### 6.3.2 Tapered Slot Antenna

The geometry of a tapered slot Vivaldi antenna is shown in Fig. 6.8. Its tapered profile is described by an exponential function. The tapered slot Vivaldi antenna is excited via the microstrip-to-slotline transition. The transition construction exploits wideband features of a microstrip radial stub used as a virtual wideband short. The microstrip is virtually shunted to the second half of the slotline metallization while the first half serves as a ground metallization for the microstrip line. It is necessary to transform the impedance of the input feeding microstrip line to the input impedance of the transition. Therefore, the linear microstrip taper is used as the input impedance transformer [132] [133]. Like the antipodal Vivaldi antenna, there is also a trade-off between the antenna size and its bandwidth towards low frequency.

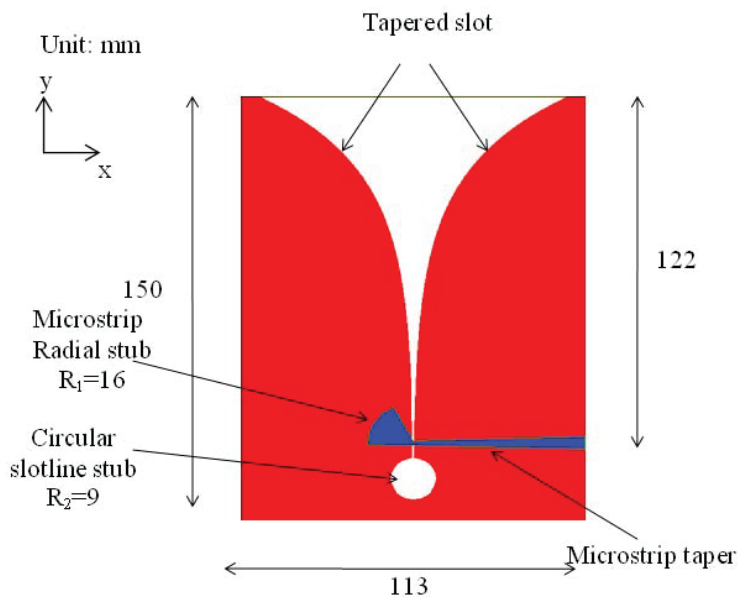
#### Measurement Results

The top and the bottom view of the fabricated tapered slot Vivaldi antenna is shown in Fig. 6.9. Measured results in Fig. 6.10 and Fig. 6.11 show that this tapered slot Vivaldi antenna presents good return loss better than -10 dB between 1 GHz and 5 GHz. This corresponds to VSWR less than 2 for operation throughout the aimed frequency band. This antenna also has a good linear phase response as displayed in Fig. 6.12. The designed antenna has small size of  $113 \times 150 \text{ mm}^2$  while the antenna in [134] has  $203 \times 292 \text{ mm}^2$ .

The measured gain values at the distance of 1 m between two identical antennas are given in table 6.2 and are plotted in Fig. 6.13. It can be seen that the gain values are higher than 8 dBi in most part of the designed frequency band in comparison with the antenna in [135] achieving a maximal gain values of 8 dBi. Fig. 6.14 displays the simulated radiation pattern of tapered slot Vivaldi antenna at 2 GHz in both the E-and H-planes achieving by Ansoft HFSS. The half-power beamwidths are  $125^\circ$  in the E-plane and  $115^\circ$  in the H-plane.



**Figure 6.7:** Simulated radiation pattern of antipodal Vivaldi antenna.



**Figure 6.8:** Structure and designed parameters of tapered slot Vivaldi antenna.

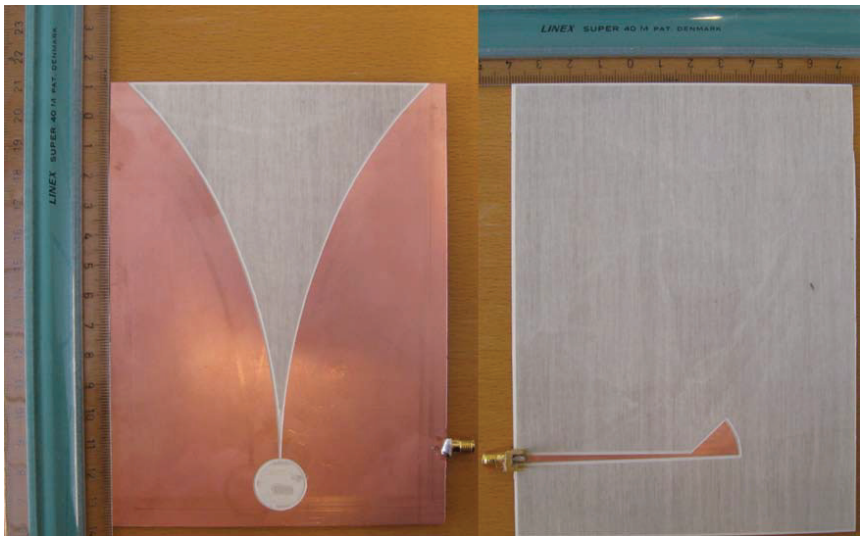


Figure 6.9: Top view and bottom view of tapered slot Vivaldi antenna.

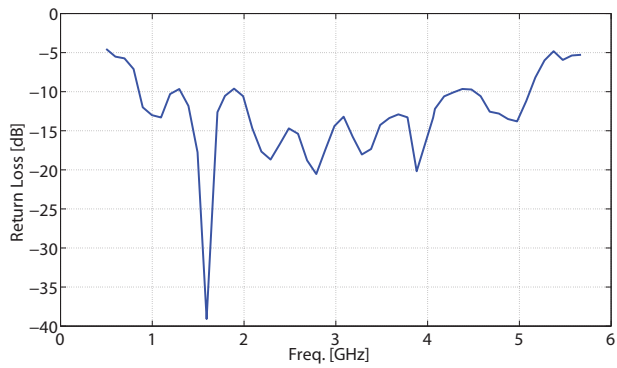


Figure 6.10: Measured return loss of tapered slot Vivaldi antenna.

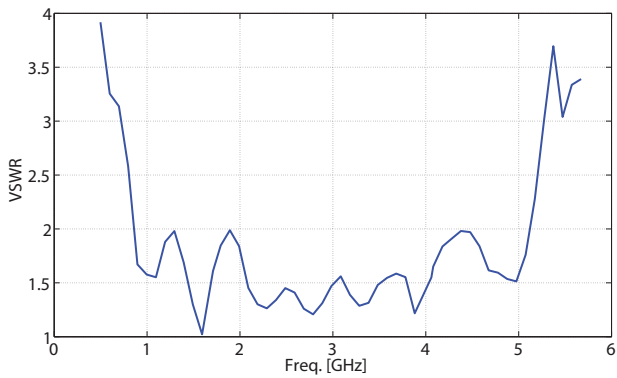
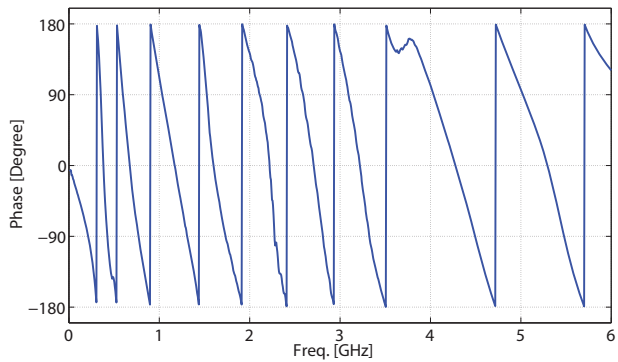


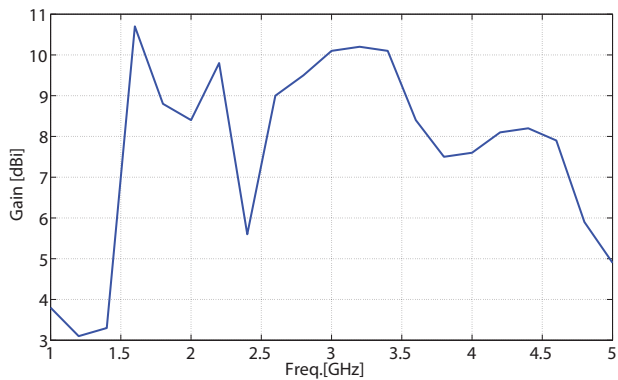
Figure 6.11: Measured VSWR of tapered slot Vivaldi antenna.



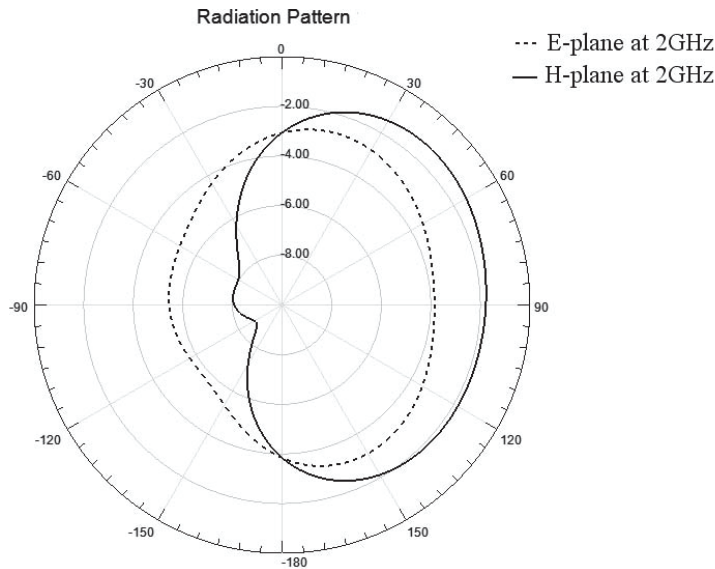
**Figure 6.12:** Measured phase response of tapered slot Vivaldi antenna.

**Table 6.2:** Measured gain values of tapered slot Vivaldi antenna.

Freq (GHz)	Gain (dBi)	Freq (GHz)	Gain (dBi)
1.00	3.80	3.20	10.20
1.20	3.10	3.40	10.10
1.40	3.30	3.60	8.40
1.60	10.70	3.80	7.50
1.80	8.80	4.00	7.60
2.00	8.40	4.20	8.10
2.20	9.80	4.40	8.20
2.40	5.60	4.60	7.90
2.60	9.00	4.80	5.90
2.80	9.50	5.00	4.90
3.00	10.10		



**Figure 6.13:** Measured gain versus frequency of tapered slot Vivaldi antenna.

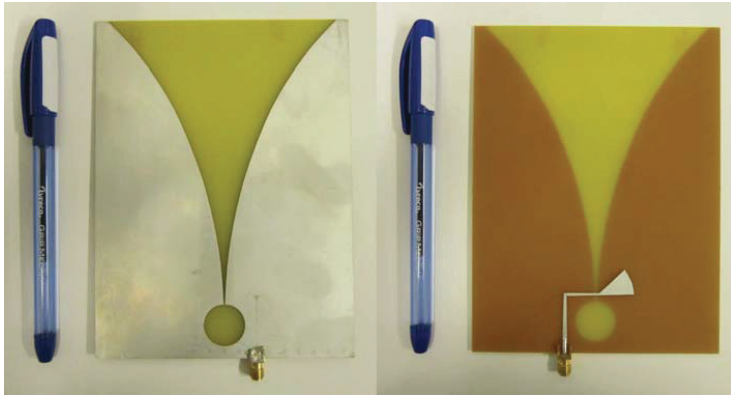


**Figure 6.14:** Simulated radiation pattern of tapered slot Vivaldi antenna.

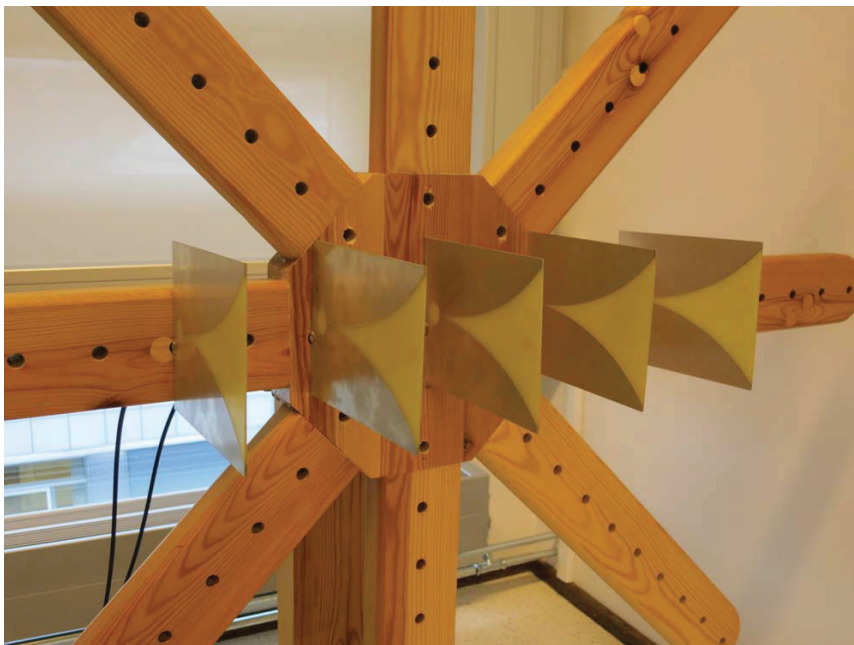
Another version of tapered slot Vivaldi antenna with feeding port on back side were fabricated on FR4 substrate as shown in Fig. 6.15. It obtains a similar performance as the one with feeding on one side. An array of this antenna have been employed in another project for measurement of a UWB beamformer as shown in Fig. 6.16.

## 6.4 Conclusion

Two types of Vivaldi antenna were designed on Rogers RO4350B substrate [Paper X]. They were both tuned for the 1–5 GHz frequency band and show significant gain. The proposed antennas show low impulse distortion and the VSWR is less than 2 over the entire bandwidth. Simulated and measured results indicate that antipodal Vivaldi antenna has to be larger than tapered Vivaldi antenna in order to achieve a similar return loss. However, a very wide bandwidth can easily achieve by the removal of the ground plane around the feeding port. Furthermore, antenna gain value will be higher with a larger antenna for both types of Vivaldi antenna. There are some trade-offs between the bandwidth and the gain as well as the size and the lower edge operating frequency of Vivaldi antennas. The wide bandwidth of Vivaldi antenna is crucial for reducing distortion. Besides, the high gain and high directivity lead to a decrease in energy consumption as the radiated energy is directed towards targets instead of transmitting in all directions.



**Figure 6.15:** Top view and bottom view of tapered slot Vivaldi antenna with feeding on back side.



**Figure 6.16:** A UWB beamformer measurement setup using tapered slot Vivaldi antennas.

## Chapter 7

# IR-UWB RECEIVER FRONT-END FOR WSN APPLICATIONS

### 7.1 Introduction

UWB technology is one of the candidates for short-range wireless communication due to its extremely large bandwidth and low emission level allowed by the Federal Communications Commission (FCC). There are two different approaches to utilize the 3.1–10.6 GHz UWB band: multiband orthogonal frequency-division multiplexing (MB-OFDM) and impulse radio (IR). The first one uses MB-OFDM modulation with fourteen 528-MHz sub-bands and a fast frequency-hopping scheme. Therefore, the carrier with a bandwidth of 528 MHz can hop to one of fourteen channels that divided into four groups of three channels and one group of two channels. MB-OFDM approach has the best potential for very high rate up to 480 Mb/s and allows for good coexistence with narrowband systems. In addition, due to the increased length of the OFDM symbol period, the modulation method can successfully reduce the effects of inter-symbol interference (ISI). Nevertheless, this robust multipath tolerance comes at the price of increased transceiver complexity, the need to combat inter-carrier interference (ICI) and tighter linear constraint on amplifying circuit elements.

On the other hand, IR is a particular form of UWB signaling in which baseband pulses of extremely short duration, typically on the order of nanosecond or sub-nanosecond, are transmitted. Therefore, the energy of the radio signal is spread over a bandwidth of several gigahertz [136]. The shape of the pulse is very important as it specifies the frequency spectrum of the transmitted signal to ensure that the maximum emitted power is within the FCC-allocated frequency mask. The information is modulated directly into the sequence of pulses. Typically, one pulse carries the information for one bit. Data could be modulated using either pulse amplitude modulation (PAM) or pulse position modulation (PPM). Multiple users can be supported using the time-hopping or direct-sequence spreading approaches. IR scheme does not require carriers or any IF processing and hence greatly reduces the transceiver complexity and overall power consumption. Therefore, IR-UWB has been increasingly popular for low power, low cost applications making it a potential candidate for WSN applications requiring low data rate, in the range of 0.1-10 Mb/s. Moreover, multi-path interference like fading can be avoided, but a major challenge is the strong

power-limitations. Due to the aforementioned benefits, IR-UWB has been selected as a physical layer by IEEE 802.15.4a for the purpose of precise ranging and low data-rate communication.

This chapter proposes an IR-UWB receiver front-end covering the frequency band of 3–5 GHz for the CTBV ranging system. All the building blocks have been presented in the previous chapters are put in together to form the proposed receiver front-end [Paper I][Paper II][Paper IV][Paper X].

## 7.2 Building Blocks

### 7.2.1 Antenna

A tapered slot Vivaldi antenna was fabricated on Rogers RO4350B substrate with a relative constant of 3.48, thickness of 1.52 mm and loss tangent of 0.0031. The antenna is first designed for the bandwidth from 1 GHz to 5 GHz. However, it is still suitable for the proposed receiver front-end. Unwanted signals received from the antenna will be filtered out by the following BPF. Measured voltage standing wave ratio (VSWR) is well below 2 over the entire of the desired bandwidth. Other characteristics of the antenna were presented in [Paper X]. Two tapered slot Vivaldi antennas have been using for communication between two CTBV ranging transceivers.

### 7.2.2 LNA

The proposed LNA topology is a cascade of CG amplifier and cascode CS amplifier. The goal is to adopt the advantages of both CGLNA and noise cancellation technique. The CS stage provides wideband input matching while the cascode CS amplifier contributes gain and cancels the first-stage noise. The input of the LNA is matched to 50  $\Omega$  enabling matching to the RX antenna. The LNA amplifies the received pulses to a suitable level for signal processing, as well as to provide enough gain to minimize the noise contribution of subsequent stages, specifically, the BPF. The LNA was designed in TSMC 90 nm CMOS. According to post-layout simulation results, The LNA achieves a peak gain of 17 dB over a -3 dB bandwidth of 3–5 GHz and a NF of 2.5–3.5 dB. It consumes 12.5 mW from a 1.2 V supply voltage and occupies an area of 0.42 mm<sup>2</sup> [Paper II].

### 7.2.3 Band-Pass Filter

Following the LNA is an inductorless tunable switched-capacitor band-pass filter based on N-path periodically time-variant networks. It is designed to reject out-of-band interferers. The filter prototype was fabricated in 90 nm CMOS and occupies a chip area of 0.004 mm<sup>2</sup>. It archives a -3 dB bandwidth of 2 GHz while the center frequency can be tuned from 4 GHz to 4.4 GHz. Power consumption is 1.1 mW from a 1.2 V supply voltage and the performance was demonstrated in [Paper I].



### 7.2.4 Quadrature Downconversion Mixer

The RF signals amplified by the LNA are then downconverted to baseband by a mixer. Down-conversion of any asymmetrically-modulated signal to a zero IF leads to self-corruption unless the baseband signals are separated by their phases, thus a quadrature mixer is necessary. The proposed quadrature mixer is a wideband modified Gilbert Cell mixer with the two quadrature pairs sharing the same input transconductor. It multiplies the received pulse with a locally template pulse generated by a quadrature voltage-controlled oscillators (QVCO). The proposed QVCO consists of two identical complementary cross-coupled LC oscillators being coupled through cascode transistors. Post-layout simulation results show that the LO frequency can be varied between 3.4 GHz and 4.6 GHz with respect to varactor control voltage. The quadrature mixer exhibits an IIP3 of 0.5 dBm at 4 GHz while the conversion gain is  $8 \pm 1$  dB and noise figure is 6-8 dB over the entire bandwidth from 1 GHz to 6 GHz. The proposed mixer consumes a total power of 6.2 mW including the QVCO dissipation and occupies an area of  $0.03 \text{ mm}^2$  while the QVCO occupies an area of  $0.2 \text{ mm}^2$  [Paper II].

### 7.2.5 Quantizer

An essential building block in the proposed IR-UWB receiver front-end is a single-bit quantizer or thresholder continuously comparing the incoming signal to a threshold voltage, giving a binary or digital output of the sign of the comparison. After I/Q downconversion, the baseband signals are amplified and quantized with a tunable threshold. The thresholding operation in the quantizer is a single-bit quantization process because the SNR is often quite low ( $<1$ ). The proposed quantizer was presented in [Paper IV]. Measurement results show that the stand-alone quantizer achieves a -3 dB bandwidth covering a spectrum from 10 MHz to 2.7 GHz. The overall gain can be varied from 23 dB to 33 dB while the NF is between 7 dB and 10 dB. The quantizer core occupies an area of  $0.04 \text{ mm}^2$  and consumes a power of 4.8 mW from a 1.2 V supply voltage.

## 7.3 Proposed IR-UWB Receiver Front-End

The proposed IR-UWB receiver front-end is depicted in Fig. 7.1 targeted for low band of UWB spectrum from 3 GHz to 5 GHz [Paper II]. It consists of an antenna, a low noise amplifier (LNA), a band-pass filter (BPF), a downconversion quadrature mixer, a low-pass filter (LPF), a differential-to-single-ended (D-to-S) converter and a single-bit quantizer. After being amplified and filtered by the LNA and BPF, respectively, the RF signal is then downconverted to baseband by the downconversion quadrature mixer. The second-order RC LPF loads the mixer further rejecting strong out-of-band interference and suppressing the high-frequency pulse signals that leak through the mixer. The signal is then fed to the D-to-S converter which performs differential to single-ended conversion and is finally quantized by the single-bit quantizer.

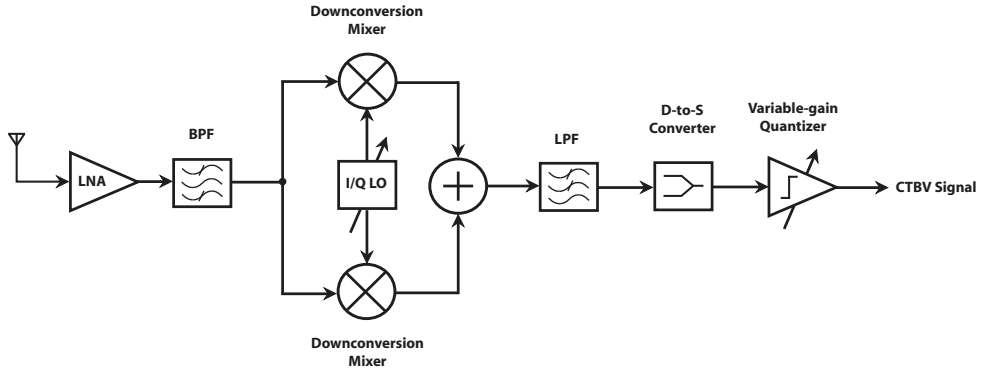


Figure 7.1: The IR-UWB receiver front-end architecture.

### 7.3.1 Post-Layout Simulation Results

The proposed IR-UWB receiver front-end has been realized in 90 nm CMOS provided by TSMC and the performance was verified by post-layout simulation. The active area is  $0.9 \text{ mm}^2$  as shown in Fig. 7.2. Fig. 7.3 plots the front-end conversion gain as a function of the RF input frequency in the highest gain mode. The receiver front-end obtains a peak gain of 45 dB over the bandwidth of 3–5 GHz. Fig. 7.4 demonstrates the performance of the front-end when a fifth derivative Gaussian pulse (Fig. 7.4a) is applied at its input. The pulse fills a bandwidth from 3.1 GHz to 5.4 GHz. The input signal is downconverted to baseband and then filtered out by the mixer and LPF, respectively, as illustrated in Fig. 7.4b. Depend on the threshold levels of the quantizer, CTBV signals should appear at the output of the receiver. When the threshold current,  $I_{th}$  is equal or smaller than  $50 \text{ }\mu\text{A}$ , the threshold is set above the input signal. As a result, the output of the receiver is always at low level (Fig. 7.4c). Conversely, when  $I_{th}$  is equal or greater than  $55 \text{ }\mu\text{A}$  corresponding to the threshold is below the input signal, the output is always at high level (Fig. 7.4h). When the threshold current is somewhere between these two values, the input signal is quantized as can be seen from Fig. 7.4d to Fig. 7.4g. The optimal threshold value for the quantizer is a trade-off between noise and shorter pulse width signals, which is an iterative process to fix. Also the dependency of temperature and process variation complicates this process. Hence the threshold is set high enough to get rid most of the noise and other ringing effects. The receiver front-end consumes a total power of 26.6 mW from a 1.2 V supply voltage. It exhibits a NF of 8–9 dB while the input return loss,  $S_{11} \leq -12 \text{ dB}$  over 3–5 GHz bandwidth. Table 7.1 summarizes the performance of the proposed receiver front-end and compares it to other published designs operating in a similar frequency range. For fair comparisons, the receiver sensitivity is normalized to 1 Mb/s at  $10^{-3}$  BER. A fully integrated low-power UWB receiver is demonstrated in [139]. It can process pulses with 500 MHz to 2 GHz bandwidth due to a variable channel select filter. In [142] a multi-stage differential inverter-based RF front end with a resonant LC load is proposed to improve energy efficiency.

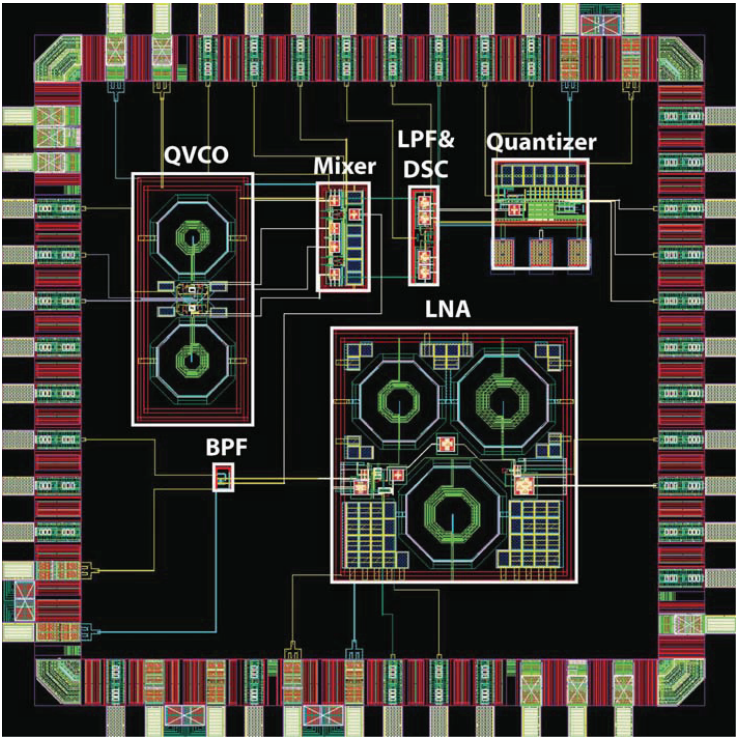


Figure 7.2: The layout of the proposed IR-UWB receiver front-end.

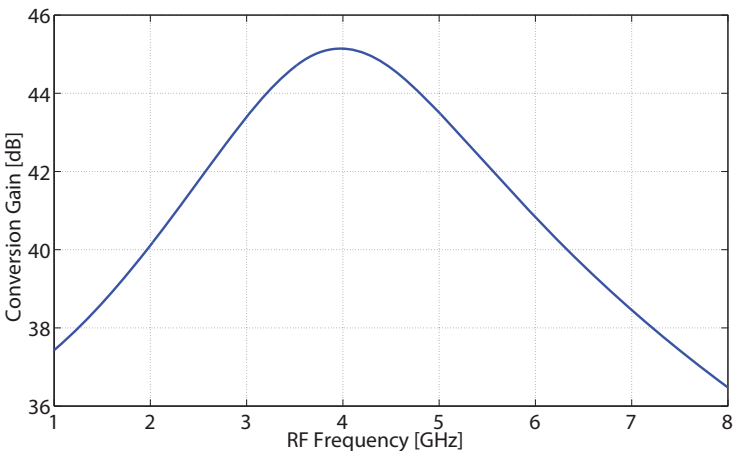
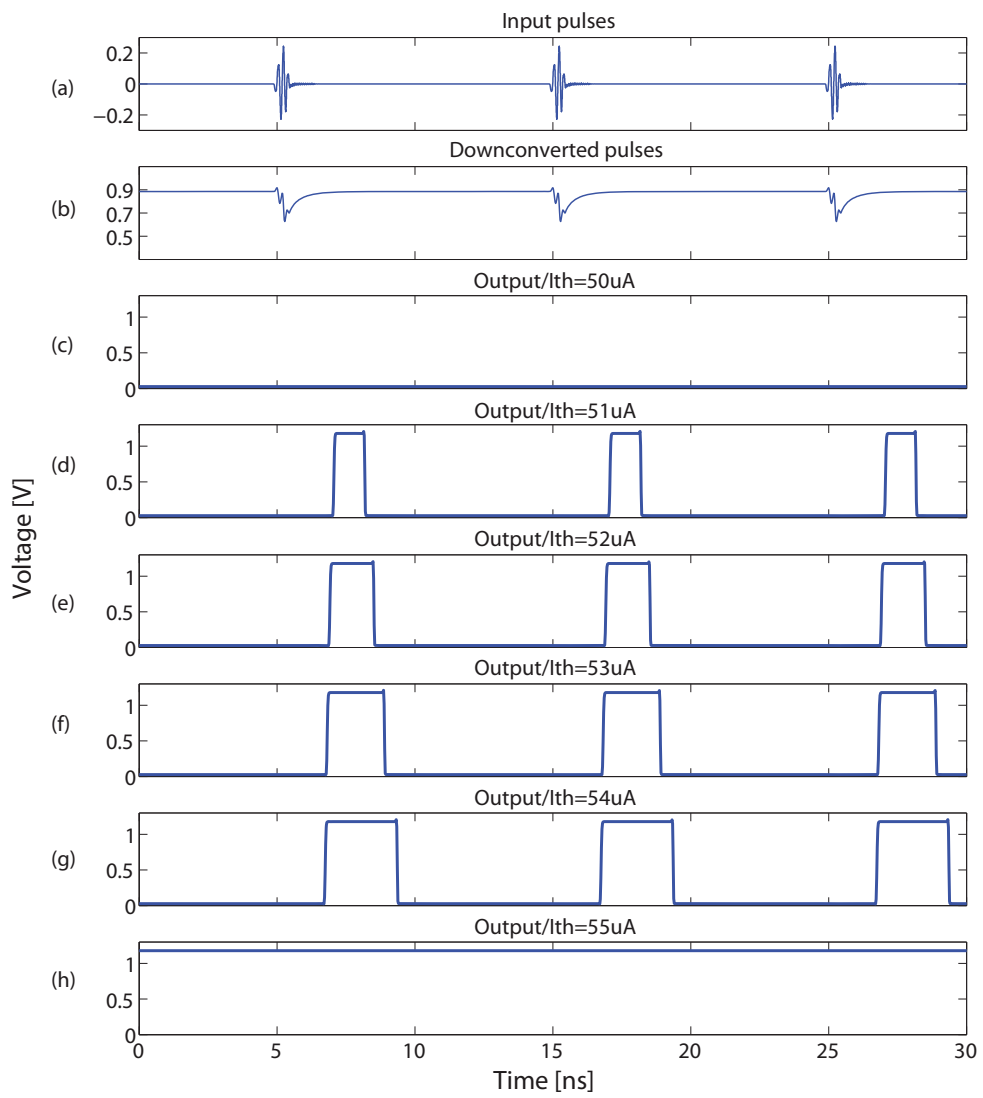


Figure 7.3: The simulated conversion gain of the IR-UWB receiver front-end in the highest gain mode.



**Figure 7.4:** The simulated performance of the proposed IR-UWB receiver front-end.

**Table 7.1:** Comparison with the previous published IR-UWB receiver front-ends

Ref.	CMOS tech.	Die area (mm <sup>2</sup> )	Power cons. (mW)	Gain (dB)	$S_{11}$ (dB)	NF (dB)	Sensitivity (dBm)
[139]	0.18 $\mu$ m	-	28.8	25	$\leq -10$	8	-
[140]	90 nm	2.2	-	40	$\leq -10$	8.6	-89
[141]	90 nm	1.1	16.3	0-18	$\leq -10$	8.5	-89
[142]	90 nm	2.25	22.5	6-45	$\leq -7.8$	7.7-9.1	-88
This work	90 nm	0.9	26.6	35-45	$\leq -12$	8-9	-89

## 7.4 Conclusion

In this chapter, we have presented a solution for IR-UWB receiver front-end targeted for low band of UWB spectrum from 3 GHz to 5 GHz [**Paper II**]. Compared to other published designs, our proposed UWB receiver front-end offer the advantage of smaller die areas, simpler designs and no external components. The proposed IR-UWB receiver front-end is highly appreciated for such applications requiring low-power low data-rate communication over relative short distances like WSNs. The performances of the proposed front-end were verified by post-layout simulation results and are competitive to other state-of-the-art IR-UWB receiver front-ends in CMOS.



# Chapter 8

## CONCLUSION AND FUTURE WORKS

### 8.1 Conclusion

Precision ranging is a key factor for localization in WSNs. Most reported ranging solutions are limited by clock frequency or clock synchronization. With the combination of CTBV technique and the IR-UWB technology, we propose a promising approach towards high precision positioning combined with communication. The main goal of this thesis is to develop an IR-UWB receiver front-end covering the frequency band of 3–5 GHz for the CTBV ranging system [**Paper II**]. The proposed IR-UWB receiver front-end has been realized in 90 nm CMOS technology intended for high-precision low-power low data-rate communication over a relative short range for WSN applications such as ranging and localization. All building blocks include antenna, LNA, band-pass filter, downconversion quadrature mixer and single-bit quantizer have been discussed in detail in previous chapters. The contributions of this work have been published in proceedings of conferences [**Paper I–X**] and can be summarized as follows

#### UWB Band-Pass Filter

Typically, off-chip passive filters like surface acoustic wave (SAW) filters are used as preselect filters in receiver front-ends. However, the demand for fully integrated systems is favouring solutions with no external components. There are various filter types that are appropriate for the implementation of RF on-chip BPFs include bulk acoustic wave (BAW) filters, active-RC filters, LC filters—often with Q-enhancement techniques,  $g_m$ -C filters and N-path filters. Each topology has distinct advantages and limitations. The N-path filter is chosen in this design since it can realize a band-pass filter whose center frequency can be tunable by simple tuning scheme. In addition, it can be implemented in inductorless configuration for saving chip area that is suitable for low-cost applications. Two solutions for SC filters based on N-path periodically time-variant networks have been demonstrated in standard 90 nm CMOS technology [**Paper I**][**Paper V**]. These filters basically transfer the low-pass characteristic of a network to a band-pass one by means of frequency mixers. As a part of the filter, novel multiphase clock generators are proposed suitable for RF frequencies. The multiphase clock generators are built with digital logic gates, thus can be easily scaled to finer pitch technology. The filter is compact, suitable for standard

digital technology and can be fully integrated without any external clock reference. This filter is competitive to other start-of-the-art tunable band-pass filters and could substitute passive SAW filters for broadband wireless radio-communication.

### **UWB Continuous-Time Single-Ended Quantizer**

An essential building block in the proposed IR-UWB receiver front-ends is a single-bit quantizer or thresholder continuously comparing the incoming signal to a threshold voltage, giving a binary or digital output of the sign of the comparison which is CTBV signal. The optimal threshold value of the quantizer is a trade-off between noise and the narrow pulse width signals. Best solution is to set the threshold high enough to get rid most of the noise and other ringing effects. Quantization performance can be obtained with a high-gain comparator. Conventional comparators are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback combined with a clocked reset, but such an approach cannot be used for continuous time systems. Four different architectures of continuous-time single-bit quantizers with tunable thresholds are proposed including both single-ended [Paper IV][Paper IX] and differential approach [Paper III][Paper VII]. By avoiding a high frequency sampling clock, power consumption is reduced and fully integrated is possible. For quantization performance, linearity is insignificant. Therefore, in the design of all quantizers, gain and noise performance are optimized trading off linearity.

### **UWB Low Noise Amplifier**

A 3–5 GHz LNA has been demonstrated in 90 nm CMOS technology [Paper II]. The input CG stage has been exploited together with noise-cancelling technique to obtain broadband input matching and noise cancellation simultaneously. The CG stage with low input impedance characteristic provides broadband impedance matching without many extra components. Using an additional auxiliary amplifier which senses the signal and noise voltage then combining the outputs of the main and the auxiliary amplifier, the thermal noise from the output of CG stage can be suppressed while simultaneously adding the signal contributions constructively. Resonant RLC loads are used instead of non-resonant loads as they offer superior gain in the 3-to-5 GHz frequencies band at the same power consumption and also have a second order band-pass characteristic which rejects out-of-band interferers.

### **Downconversion Quadrature Mixer**

Linearity requirement has a large impact on the choice of mixer topologies. When linearity considerations are insignificant, Gilbert Cell mixers can be employed instead of other topologies for superior noise and gain characteristics. A modified Gilbert Cell mixer with two quadrature pairs sharing the same input transconductor was designed using TSMC 90 nm CMOS technology [Paper II]. Compared to double-balanced Gilbert Cell based mixer adopting two separate transconductors, this proposed mixer allows a higher switching pair current gain. In addition, the parasitic capacitance loading the previous stage is minimized for the same transconductance



gain. The choice of a single-balanced topology instead of its double-balanced alternative is due to the following reasons. First, this avoids a single-to-differential converter required after the LNA, which increases power consumption. Second, the single-balanced architecture introduces less input-referred noise compared to double-balanced one. Along with the mixer is an on-chip QVCO based on two complementary cross-coupled LC oscillators. The complementary configuration is exploited to increase the amplitude oscillation as well as reduce phase noise.

### UWB Antennas

UWB systems without any carriers require special considerations for antenna design. From a systems point of view, UWB antenna systems should transmit and receive high-quality signals for high SNR at a receiver. For impulse radio systems, distorted waveforms of received pulses at a receiver will degrade the SNR. Two different types of UWB Vivaldi antenna were fabricated on Rogers RO4350B substrate for 1–5 GHz frequency band [Paper X]. Both antennas reveal small distortion on the transmission of fifth derivative Gaussian pulse. In the design of the antipodal Vivaldi antenna, the ground plane around the feeding port is removed to increase the impedance bandwidth without changing the radiation pattern. The tapered slot Vivaldi antennas are designed with feeding port on one side and feeding port on back side suitable for different applications.

## 8.2 Future Works

The importance of localization or positioning in WSN nodes is currently an important research topic. The CTBV ranging system is still in its infancy, thus there is probably several undiscovered ways to improve it. One of the way is improving the IR-UWB receiver front-end. In the following, a brief list of specific topics that may be investigated further is given.

### UWB Continuous-Time Single-Ended Quantizer

To overcome the conventional limits on bandwidth, several bandwidth enhancement techniques using inductors can be utilized trading off chip areas and peaking in the magnitude responses. From the other hand, during measurement of the differential quantizer [Paper III], it sometimes exhibits instability when the two outputs were at rail voltages. This phenomenon may be caused by DC offset as a result of device mismatch between the two MOSFETs of the differential pair or the asymmetry in the layout for two paths of the differential signals. Therefore, in the cascade of direct-coupled amplifiers, the DC offset may drive the following stages out of linear operation. The DC offset also limits the minimum signal level that can be detected. The differential quantizer performance can be improved by applying an offset cancellation technique.

Besides, alternative thresholding solutions like automatic thresholding can be explored instead of linear sweeps. An automatic-threshold differential quantizer is proposed in Fig. 8.1. In this configuration, the differential thresholds are set automatically by the feedback loops to ensure that only 1% of the input signal level will pass the threshold.



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# Appendix A

## List of Publications

1. **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess and T. S. Lande, "*An Inductorless 3-5 GHz Band-Pass Filter with Tunable Center Frequency in 90 nm CMOS*," The 2013 IEEE International Symposium on Circuits and Systems (ISCAS 2013), pp. 1-4, May 2013.
2. **T. A. Vu**, H. A. Hjortland, O. Naess and T. S. Lande, "*A 3-5 GHz IR-UWB Receiver Front-End for Wireless Sensor Networks*," The 2013 IEEE International Symposium on Circuits and Systems (ISCAS 2013), pp. 1-4, May 2013.
3. **T. A. Vu** and T. S. Lande, "*A Continuous-Time Differential Single-Bit Quantizer for IR-UWB Receivers*," The 2013 IEEE International Conference on Ultra Wideband (ICUWB 2013), pp. 1-4, September 2013, *accepted*.
4. **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*A Variable-Gain Single-Bit Ultra-Wideband Quantizer for Baseband Receiver Front-End*," The 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2012), pp. 483-486, December 2012.
5. **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*An Inductorless 6-Path Band-Pass Filter with Tunable Center Frequency for UWB Applications*," The 2012 IEEE International Conference on Ultra Wideband (ICUWB 2012), pp. 164-167, September 2012.
6. **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*An Ultra-Wideband, Continuous-Time, Differential, Single-Bit Quantizer in 90 nm CMOS*," The 54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2011), pp. 1-4, August 2011.
7. **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*A 70-dB, 3.1-10.6-GHz CMOS Amplifier in Low-Power 90 nm CMOS*," The 54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2011), pp. 1-4, August 2011.
8. **T. A. Vu**, S. Sudalaiyandi, M. Z. Dooghabadi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*Continuous-Time CMOS Quantizer for Ultra-Wideband Applications*," The 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010), pp. 3757-3760, May 2010.



9. **T. A. Vu**, S. Sudalaiyandi, M. Z. Dooghabadi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*UWB Vivaldi Antenna for Impulse Radio Beamforming*," The 27th Norchip conference, pp. 1-5, November 2009.

**CO-AUTHOR:**

10. S. Sudalaiyandi, H. A. Hjortland, **T. A. Vu**, O. Naess and T. S. Lande, "*Continuous-Time High-Precision IR-UWB Ranging-System in 90 nm CMOS*," The 2012 IEEE Asian Solid State Circuits Conference (A-SSCC 2012), pp. 1-4, November 2012.

11. S. Sudalaiyandi, **T. A. Vu**, H. A. Hjortland, O. Naess and T. S. Lande, "*Continuous-Time Symbol Detector for IR-UWB Rake Receiver in 90 nm CMOS*," The 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2012), pp. 487-490, December 2012.

12. S. Sudalaiyandi, H. A. Hjortland, **T. A. Vu**, O. Naess and T. S. Lande, "*Live Demonstration: IR-UWB Transceiver with Localization Based on ToF Technique Suitable for Wireless Capsule Endoscopy*," The 2012 IEEE Biomedical Circuits and Systems Conference (BioCAS 2012), November 2012.

13. S. Sudalaiyandi, **T. A. Vu**, H. A. Hjortland, O. Naess and T. S. Lande, "*Continuous-Time Single-Symbol IR-UWB Symbol Detection*," The 2012 IEEE International System-on-Chip Conference (SoCC 2012), pp. 198-201, September 2012.

14. S. Sudalaiyandi, M. Z. Dooghabadi, **T. A. Vu**, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*Power-Efficient CTBV Symbol Detector for UWB Applications*," The 2010 IEEE International Conference on Ultra Wideband (ICUWB 2010), pp. 1-4, September 2010.

15. M. Z. Dooghabadi, **T. A. Vu**, S. Sudalaiyandi, H. A. Hjortland, O. Naess, T. S. Lande and S. E. Hamran, "*Electromagnetic Impulse Radio Camera*," The 27th Norchip conference, pp. 1-5, November 2009.



**Paper I: An Inductorless 3-5 GHz Band-Pass Filter with Tunable  
Center Frequency in 90 nm CMOS  
IEEE ISCAS 2013**

The 2013 IEEE International Symposium on Circuits and Systems, pp. 1-4, May 19-23, 2013,  
Beijing, China.



# An Inductorless 3–5 GHz Band-Pass Filter with Tunable Center Frequency in 90 nm CMOS

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**Abstract**—A novel inductorless tunable switched-capacitor band-pass filter based on N-path periodically time-variant networks is presented. The proposed UWB band-pass filter is complete with ring-oscillator used for multi-phase clock generation suitable for power-efficient IR-UWB systems. The filter prototype was fabricated in TSMC 90 nm CMOS, and occupies a chip area of 0.004 mm<sup>2</sup>. It archives a -3 dB bandwidth of 2 GHz while the center frequency can be tuned from 4 GHz to 4.4 GHz. Power consumption is 1.1 mW from 1.2 V supply voltage, and the performance was verified experimentally.

**Index Terms**—Band-Pass Filter, Frequency Tuning, Multiphase Clock, N-Path Filter, Switched-Capacitor Circuits, UWB Filter.

## I. INTRODUCTION

As wireless communication is moving up to higher frequencies, suitable integrated band-pass filters (BPFs) are required. Typically passive filters like surface acoustic wave (SAW) filters are used. Aiming at integrated filter solutions, SAW-filters are not viable [1]. An additional challenge is wideband, microwave filters for impulse radio applications. At microwave frequencies, wideband resonator based filters are hard to make and area consuming. Recently, there has been a renewed interest in switched-capacitor (SC) N-path filters due to the development of CMOS technology allowing this type of filter to work at RF frequencies [2][3]. They are also known as sampled data filters, commutated capacitors, etc. These filters basically transfer the low-pass/notch characteristic of a network to a band-pass/band-stop one by means of frequency mixers. An N-path filter can realize an inductorless tunable band-pass or band-stop filter in which the center frequency is determined by the mixing frequency. They have been widely utilized in receivers to replace SAW filters in low-cost wireless radio-communication applications. In addition to cost implications, these SAW filters not only degrade the receiver sensitivity due to their inevitable insertion loss, they are also hard to make tunable. Furthermore, the demand for fully integrated systems is favouring solutions with no external components achievable with novel receiver architectures as well as novel circuit topologies. SC circuits achieve high transfer-function accuracy with low distortion in CMOS technology and thus become attractive for low-voltage operation. A combination of SC filter and N-path technique allows realization of high-quality RF filters even with simple ring-oscillators as multi-phase clock generators. Still a major challenge is to generate a high-speed multi-phase clock suitable for microwave filtering.

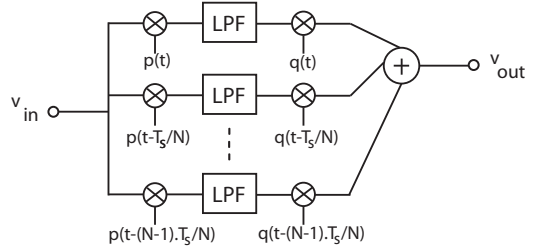


Fig. 1. The structure of an N-path filter.

## II. PRINCIPLES OF SC N-PATH FILTERS

A typical N-path filter is composed of N parallel identical filter cells which are cyclically sampled with the frequency  $F_s$ . Each path usually in turn consists of a passive low-pass filter (LPF) with transfer function  $H(f)$  between an input and output mixer as shown in Fig. 1. The switches are driven by time/phase shifted versions of clock  $p(t)$  and  $q(t)$ . The time shift between two successive paths is  $T_s/N$ , where  $T_s$  is the period of the mixer clock. At any moment one and only one path is connected to the output node. When the switching signals are assumed to be ideal Dirac impulses delayed by  $T_s/N$ , the output signal  $S(f)$  may be written as a function of the input signal  $E(f)$  as shown in equation (1).

$$S(f) = \sum_{m=-\infty}^{+\infty} h(m \cdot T_s) \cdot \exp(-2 \cdot \pi \cdot j \cdot f \cdot m \cdot T_s) \quad (1)$$

$$\cdot \sum_{n=-\infty}^{+\infty} e\left(\frac{n \cdot T_s}{N}\right) \cdot \exp(-2 \cdot \pi \cdot j \cdot f \cdot \frac{n \cdot T_s}{N})$$

Equation (1) shows that the output signal is the result of two multiplied sums. The first term corresponds to the Fourier transform of the impulse response of the low-pass filter sampled at  $T_s$  period. The second one corresponds to the Fourier transform of the input signal sampled at  $T_s/N$  period. Due to the periodicity of the frequency response, the band-pass center frequency is equal to a multiple of the clock frequency. This filter can be used for clock recovery by filtering the harmonic components [4]. It can also be used as band-pass filter centered around  $F_s$  [1]. Thus, the N-path filter transfers a

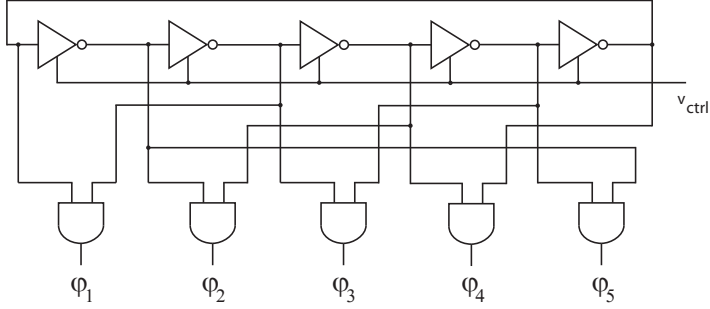


Fig. 2. The proposed 5-phase clock generator.

low-pass characteristic to a band-pass whose center frequency is controlled by the clock frequency while the low-pass filter and duty cycle of the clock define the bandwidth. In fact the input signal is downconverted to baseband, filtered, and then upconverted again to the same band as the input signal. A multi-phase clock generator with wide tuning-range is required for center frequency tuning.

### III. DESIGN OF A UWB SC 5-PATH BAND-PASS FILTER

#### A. Low-Pass Filter

As mentioned before, the roll-off and bandwidth of the N-path band-pass filter is determined by the sharpness of the low-pass filter. For most wideband filters a second-order passive low-pass filter is sufficient. A second-order RC low-pass filter is designed for improved frequency roll-off. Thus, the gain decreases by 40 dB per decade above cut-off frequency. Besides, the RC in each path of an N-path filter performs integration on the input signal when the corresponding switch is on. Any variation of R and C will result in filter bandwidth deviations from the designed value.

#### B. Multi-Phase Clock Generator

Since the center frequency of the SC N-path band-pass filter can be tuned with the clock frequency, a high-speed tunable oscillator is desirable. The tunability is particularly useful for RF integrated circuits, for which the tuning of the center frequency by a clock signal permits either to compensate for process variations and device mismatch or to filter various channels with the same filter. Several clock generator topologies for RF frequencies have been proposed in literature [5]. Most of them use inductors and capacitors to provide oscillation. These inductors occupy a very large area in the layout and are hard to adapt to finer pitch technology. In this design, a ring oscillator based, multi-phase clock generator is proposed. Avoiding an external crystal-driven clock, higher frequencies are feasible and full integration is possible. The multi-phase clock generator is built with digital logic gates and can be scaled with CMOS technology as shown in Fig. 2. Five inverters form a closed loop with positive feedback. It generates a 5-phase clock signal used for driving SC circuits.

In order to tune the oscillation frequency, a programmable delay is provided by tuning the back-gate (bulk) voltage of the PMOS devices of the inverters in the ring. In this way no additional loading is applied, thus, maintaining the highest possible oscillator frequency. Both back-gate voltages of NMOS transistor and PMOS transistor can be controlled, but it would require two different voltage levels dependent on each other, which is difficult to accomplish.

The intrinsic propagation delays of each inverter are

$$t_{\text{PHL-INV}} = 0.7R_N C_{\text{load}} \quad (2)$$

$$t_{\text{PLH-INV}} = 0.7R_P C_{\text{load}} \quad (3)$$

Where  $t_{\text{PHL-INV}}$  and  $t_{\text{PLH-INV}}$  are the high-to-low and low-to-high delay of the inverter,  $R_N$  and  $R_P$  are the equivalent resistances of the NMOS transistor and PMOS transistor, respectively, and  $C_{\text{load}}$  is the load capacitance on the output of each inverter. The oscillation frequency,  $w_0$ , is given by

$$w_0 = \frac{2\pi}{5(t_{\text{PHL-INV}} + t_{\text{PLH-INV}})} \quad (4)$$

The phase noise of the ring oscillator is investigated in [6], an can be calculated as

$$L(\Delta\omega) = A_k \frac{kTR_{\text{ns}}}{V_A^2} \left( \frac{w_0}{\Delta\omega} \right)^2 \quad (5)$$

Where  $A_k$  is a factor depending on the noise generation mechanism studied,  $k$  is the Boltzmann's constant,  $T$  is the temperature in Kelvin,  $R_{\text{ns}}$  is an equivalent noisy resistor,  $V_A$  is the voltage amplitude of the signal, and  $\Delta\omega$  is the frequency offset. In order to reduce the phase noise, the equivalent resistance  $R_{\text{ns}}$  must be reduced trading off against increase in power consumption.

#### C. Proposed UWB SC 5-Path Band-Pass Filter

Fig. 3 shows the proposed SC 5-path band-pass filter. It consists of five low-pass filters, and each low-pass filter is connected to an input switch driven by a 20% duty-cycle periodic clock. The switches are made with NMOS transistors, which are switching sequentially between the ON and OFF modes. The NMOS switch passes a small signal well while

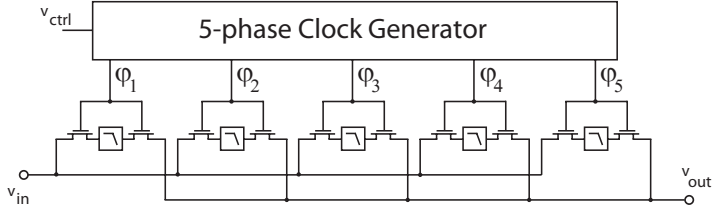


Fig. 3. The proposed UWB SC 5-path band-pass filter.

the PMOS switch passes a large signal well. In addition, input signal to the band-pass is much smaller than supply voltage. Therefore, the NMOS switch is chosen in this design instead of PMOS switch for maximizing input/output signal range when body effect is taken into account. Combining the NMOS and PMOS into a transmission gate (TG) can pass well both large and small signal at the price of larger layout area and need for two complementary clocks. Switch resistance can have strong impact on the maximum achievable rejection in N-path filters. In order to increase the maximum rejection of the filter, the switch resistance should be very small with respect to the source resistance. Increasing switch size will improve linearity, and decrease the switch resistance. However, larger switch size also means larger parasitic capacitors, affecting the frequency range, clock leakage, and also requiring more clock power to drive the switches [3]. From the other hand, the propagation delays of the NMOS switch is estimated as

$$t_{\text{PHL-SW}} = t_{\text{PLH-SW}} = 0.7R_{\text{sw}}C_{\text{tot}} \quad (6)$$

Where  $t_{\text{PHL-SW}}$  and  $t_{\text{PLH-SW}}$  are the high-to-low and low-to-high delay of the switch, respectively,  $R_{\text{sw}}$  is the switch resistance of the NMOS switch, and  $C_{\text{tot}}$  is the total capacitance on the output of the switch, that is, the sum of the output capacitance, any capacitance of interconnecting lines, and the input capacitance of the following stages. Increasing switch size reduces the propagation delays from the input to the output of the switch. However, the delay in turning the switch on is increased due to higher input capacitance. Therefore, the sizes of the NMOS switches were optimized during simulation.

#### IV. MEASUREMENT RESULTS

In order to verify the performance of the filter, a chip prototype was implemented in TSMC 90 nm CMOS. Fig. 4 shows the die microphotograph of the proposed filter. The filter core occupies an area of only  $0.075 \times 0.055 \text{ mm}^2$ . Due to the filling structures, the planarization of metal layers and the passivation layer in this 90 nm CMOS technology, the chip photo does not show any details of the circuitry. Fabricated dies were bonded directly to FR4 PCBs to avoid the inductive load of a package and to avoid long bond wires. The input of the filter was matched to  $50 \Omega$  for measurement purpose. Input RF interface was connected to SMA connector. Adopted  $50 \Omega$  transmission line, the RF signal path was carefully designed and isolated. The output of the filter was measured

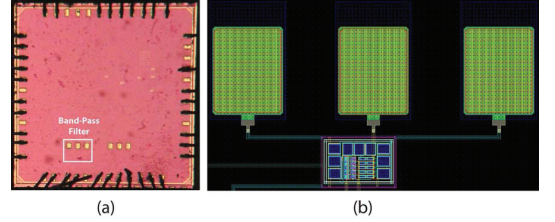


Fig. 4. The die microphotograph (a) and the layout (b) of the proposed band-pass filter.

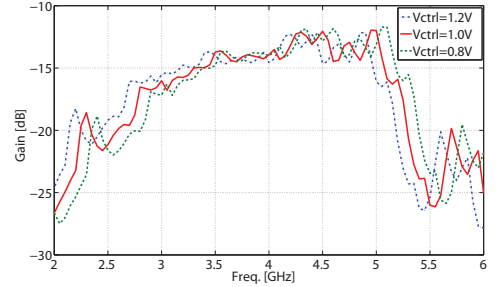


Fig. 5. The measured filter responses at different center frequencies.

by means of on-chip probing. The probe pads were designed for ground-signal-ground (GSG) probes with  $100 \mu\text{m}$  pitch. A Rohde & Schwarz ZVB20 vector network analyzer was used for measuring S-parameters as well as phase responses. In this technology, operation center frequency up to 4.4 GHz can be expected. The filter responses at different switching frequencies are plotted in Fig. 5. Tuning the back-gate bias voltage of the PMOS devices in the ring oscillator results in a frequency tuning range of 9.5% around 4.2 GHz.

Fig. 6 demonstrates the phase behaviour of the filter. As can be seen, the filter expresses a linear phase shift over the designed band between 3 GHz and 5 GHz. The phase linearity ensures minimal dispersive distortion of UWB pulses. The distortion is then verified again by applying a fifth derivative Gaussian pulse at the input of the filter, and then looking at the output signal on an oscilloscope. The pulse fills a bandwidth from 3.1 GHz to 5.4 GHz, and as expected, no dispersion is

TABLE I  
COMPARISON WITH PREVIOUS PUBLISHED TUNABLE BAND-PASS FILTER

Parameter	[3]	[1]	[7]	[8]	[9]	[10]	This work
CMOS technology	65 nm	0.35 $\mu\text{m}$	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	0.5 $\mu\text{m}$	0.5 $\mu\text{m}$	90 nm
Die area ( $\text{mm}^2$ )	0.07	1.9	0.81	0.1	0.15	2.5	0.004
Power cons. (mW)	2–16	63	17	5	43.2	15	1.1
Voltage Gain (dB)	-2	-2	0	-5	-15	23	-12
-3 dB bandwidth	35 MHz	1.75–4.6 MHz	130 MHz	53.8 MHz	80 MHz	70 MHz	2 GHz
Freq. tuning range	0.1–1 GHz	240–530 MHz	2–2.06 GHz	1.93–2.19 GHz	1.77–1.86 GHz	2.45–2.85 GHz	4–4.4 GHz
Noise figure (dB)	3–5	9	15	26.8	28	6	14

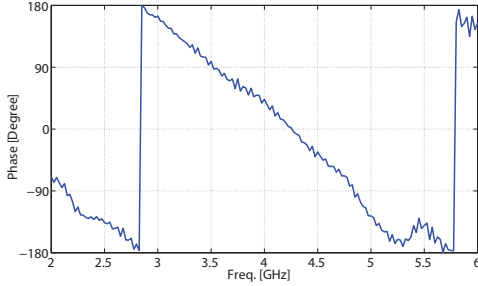


Fig. 6. The measured phase response.

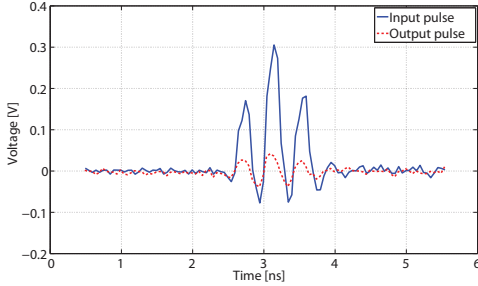


Fig. 7. Input/output fifth derivative Gaussian pulse.

added by the filter when the main part of the output pulse is well preserved. Both input and output signal are plotted in Fig. 7 indicating some attenuation of the filtered signal. The noise performance was measured by gain method using a Rohde & Schwarz FSQ26 signal analyzer. It reveals that the NF is approximately 14 dB. This high NF is due to the high filter's insertion loss as a result of input mismatching. The wideband filter consumes a power of 1.1 mW from a 1.2 V supply voltage. Table I summarizes the performance of the filter, and compares it to other previous published tunable band-pass filter in CMOS. This filter offers the smallest area and highest center frequency of all the filters reported in table I.

## V. CONCLUSION

In this paper, we have presented an inductorless SC 5-path band-pass filter targeted for low band of the UWB spectrum.

The filter occupies a chip area of  $0.004 \text{ mm}^2$ , and consumes a power of 1.1 mW from 1.2 V supply voltage. It achieves a -3 dB bandwidth of 2 GHz with center frequency tuning range between 4 GHz and 4.4 GHz. NF is approximately 14 dB over 3–5 GHz bandwidth with minimal dispersion. The filter is compact, suitable for standard digital technology, and can be fully integrated without any external clock reference. This filter is competitive to other start-of-the-art tunable band-pass filters, and could substitute passive SAW filters for broadband wireless radio-communication.

## ACKNOWLEDGMENT

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**Paper II: A 3-5 GHz IR-UWB Receiver Front-End for Wireless  
Sensor Networks  
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# A 3–5 GHz IR-UWB Receiver Front-End for Wireless Sensor Networks

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**Abstract**—This paper presents a impulse-radio ultra-wideband (IR-UWB) receiver front-end covering the frequency band of 3–5 GHz intended for low power, low data-rate communication over a relative short range for such applications like wireless sensor networks (WSNs). The receiver front-end was designed and verified in 90 nm CMOS provided by TSMC. It employs direct-conversion (homodyne) architecture, and occupies a chip area of 0.9 mm<sup>2</sup>. The receiver exhibits a peak gain of 45 dB at 4 GHz, and consumes a total power of 26.6 mW from a 1.2 V supply voltage. Input return loss,  $S_{11} \leq -12$  dB, and noise figure (NF) is between 8 dB and 9 dB through 3–5 GHz bandwidth.

## I. INTRODUCTION

Ultra-Wideband (UWB) technology is one of the candidates for short-range wireless communication due to its extremely large bandwidth and low emission level allowed by the Federal Communications Commission (FCC). There are two different approaches to utilize the 3.1–10.6 GHz UWB band: multiband orthogonal frequency-division multiplexing (MB-OFDM), and IR-UWB. Impulse radio (IR) is a particular form of UWB signaling in which baseband pulses of extremely short duration, typically on the order of nanosecond or sub-nanosecond, are transmitted. Therefore, the energy of the radio signal is spread over a bandwidth of several gigahertz. The shape of the pulse is very important as it specifies the frequency spectrum of the transmitted signal to ensure that the maximum emitted power is within the FCC-allocated frequency mask. IR-UWB has been increasingly popular for low power, low cost applications make it a potential candidate for WSN applications requiring low data rate, in the range of 0.1–10 Mb/s. Moreover, multipath interference like fading can be avoided, but a major challenge is the strong power-limitations.

## II. IR-UWB RECEIVER ARCHITECTURE

The IR-UWB receiver front-end is proposed in Fig. 1 targeted for low band of UWB spectrum from 3 GHz to 5 GHz. It consists of an antenna, a low noise amplifier (LNA), a band-pass filter (BPF), a downconversion quadrature mixer, a low-pass filter (LPF), a differential to single-ended (D-to-S) converter, and a single-bit quantizer. After being amplified and filtered by the LNA and BPF, respectively, the RF signal is then downconverted to baseband by the downconversion quadrature mixer. The second-order RC LPF loads the mixer further rejecting strong out-of-band interference and suppressing the high-frequency pulse signals that leak through the mixer. The signal is then fed to the D-to-S converter which performs differential to single-ended conversion and is finally

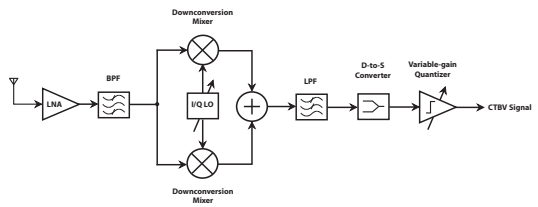


Fig. 1. The proposed IR-UWB receiver front-end architecture.

quantized by the single-bit quantizer. This paper will discuss in detail about the design of the LNA and the downconversion quadrature mixer while the analysis and measurement results of the stand-alone blocks like antenna, BPF, and quantizer were published earlier.

### A. LNA

Fig. 2 shows the schematic of the proposed LNA. It consists of a CG input stage followed by two parallel CS stages that perform noise cancellation. The goal is to adopt the advantages of both CGLNA and noise cancellation technique. The CG topology is chosen for input matching due to the following reasons. First, the CG stage with low input impedance characteristic and broadband behaviour provides NF that is almost independent of the frequency of operation. Besides, the CG stage also eliminates the Miller effect, hence, provides better isolation from the output return signal. However, a single-stage CG amplifier may not have sufficient gain, therefore, a cascade of CG amplifier and cascode CS amplifier has been used to increase the gain. The parasitic inductance of bond wire,  $L_{\text{bond}}$ , and parasitic capacitances  $C_{\text{pad}}$ ,  $C_{\text{ESD}}$ , of the bond pad and the ESD protection, respectively, have been taken into account in the design of the proposed LNA. Usually, 1 mm bond wire provides 1 nH inductance. Absorbing parasitic capacitances is relatively simple, and is less effected by process variations in the case of the CG topology. The LNA is intended for IR-UWB systems, thus, the input matching network needs to have a flat group delay across the passband to keep the distortion of the pulse shape at minimum. The shunt branch inductor,  $L_S$ , facilitates the DC biasing by sinking the common drain current of  $M_1$  to the circuit ground. The size of  $M_3$  is designed for the output bandwidth of the first stage. The LNA can be stabilized by maximizing their reverse isolation,

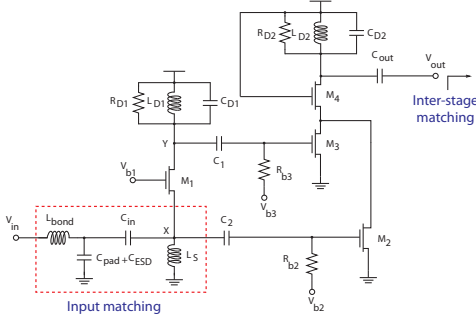


Fig. 2. The proposed LNA.

thus, adding the cascode transistor  $M_4$  further improves input-output reverse isolation and stability. It also increases the low frequency gain and reduces the input capacitance of the second stage by decreasing the Miller effect due to  $M_3$ .  $C_1$ ,  $C_2$ ,  $C_{in}$ , and  $C_{out}$  block the DC offset while  $R_{b2}$  and  $R_{b3}$  establish proper biases. Two parallel RLC tanks resonate at different frequency shaping the bandwidth of the LNA. Resonant RLC loads are used instead of non-resonant loads as they offer superior gain in the 3-to-5 GHz frequencies band at the same power consumption and also have a second order band-pass characteristic which rejects out-of-band interferers [1]. On-chip inductors  $L_{D1}$ ,  $L_{D2}$ , and  $L_S$  have a value of 2, 1.9, and 3 nH, respectively.

For simplicity of the analysis, the body effects of the MOS devices are ignored. Based on the small-signal model, the input impedance of the LNA can be derived as

$$Z_{in} = \frac{r_{ds1} + Z_L}{1 + g_{m1}r_{ds1}} \parallel sL_{bond} + \frac{1}{s(C_{pad} + C_{ESD})} \parallel sL_S + \frac{1}{sC_{in}} \parallel \frac{1}{sC_{gs1}} \quad (1)$$

Where  $r_{ds1}$ ,  $g_{m1}$ , and  $C_{gs1}$  are the drain-source resistance, transconductance, and gate-source capacitance, of  $M_1$ , respectively.  $Z_L$  is the load impedance looking from the drain of  $M_1$ . The noise voltages at nodes X and Y are converted to currents by  $M_2$  and  $M_3$ , respectively. By properly designing  $g_{m2}$  and  $g_{m3}$ , the noise contributed by  $M_1$  can be cancelled at the output. The condition for complete noise cancellation is derived in [2]. By applying the noise-cancelling technique, the noise factor is now dominated by  $R_{D1}$ ,  $M_2$ , and  $M_3$ . The total noise factor F is approximated as

$$F = \frac{R_S}{R_{D1}} + \frac{R_S}{R_{D1}} \frac{\gamma}{\alpha} \frac{1}{g_{m2}R_{D1}} + \frac{\gamma}{\alpha} \frac{1}{g_{m3}R_S} \quad (2)$$

Where  $R_S$  is the source impedance,  $\alpha = g_m/g_{d0}$ ,  $g_{d0}$  is the channel conductance for  $V_{DS} = 0$ , and  $\gamma$  is a noise parameter.

The LNA was designed in TSMC 90 nm CMOS. According to post-layout simulation results, the proposed LNA occupies an area of only 0.4 mm<sup>2</sup>. It obtains a peak gain of 17 dB, a NF of 2.5–3.5 dB over the entire -3 dB bandwidth from

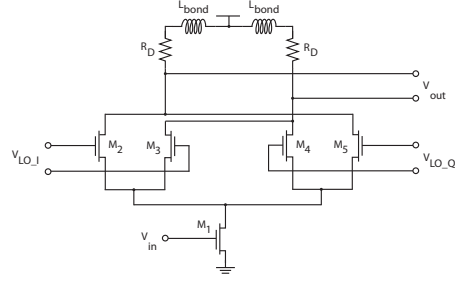


Fig. 3. The proposed downconversion quadrature mixer.

3 GHz to 5 GHz, and an IIP3 of -8 dBm, while consuming 12.5 mW from a 1.2 V supply voltage.

### B. Proposed Downconversion Quadrature Mixer

The RF signals amplified by the LNA are then down-converted to baseband by a mixer. Downconversion of any asymmetrically-modulated signal to a zero IF lead to cancellation unless the baseband signals are separated by their phases thus a quadrature mixer is necessary. In addition, linearity requirement has a large impact on the choice of mixer topologies. When linearity considerations are insignificant, Gilbert Cell mixers can be employed instead of other topologies for superior noise and gain characteristics. The quadrature mixer is proposed in Fig. 3. It is a wideband modified Gilbert Cell mixer. A single common-source transconductor ( $M_1$ ) injects the RF signal in two single-balanced quadrature commutating pairs. Compared to double-balanced Gilbert Cell based mixer adopting two separate transconductors, this proposed mixer allows a higher switching pair current gain [3]. Besides, the parasitic capacitance loading the previous stage is minimized for the same transconductance gain. The choice of a single-balanced topology instead of its double-balanced alternative is due to the following reasons. First, this avoids a single-to-differential converter which increases power consumption. Second, the single-balanced architecture introduces less noise compared to double-balanced one [4]. Bond wire inductances have been exploited for bandwidth enhancement.

The mixer is driven by quadrature clock signals, which are generated by a quadrature voltage-controlled oscillator (QVCO). The proposed QVCO, depicted in Fig. 4, is composed of two identical complementary cross-coupled LC oscillators coupled through cascode transistors. The cascode topology creates a phase delay which moves the QVCO operation away from the unstable boundary, thereby giving QVCO adequate phase margin to ensure the VCO stays in a stable mode, ultimately eliminating bimodal oscillation [5]. The complementary cross-coupled LC oscillator has been exploited in this design. Firstly, by reusing the current of NMOS transistor for PMOS transistor, the total transconductance is  $g_{mn} + g_{mp}$  compared to just  $g_{mn}$  of a non-complementary VCO with the same current. Where  $g_{mn}$  and  $g_{mp}$  are the transconductance of



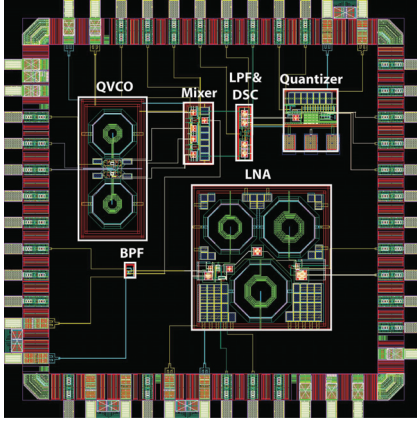


Fig. 5. The layout of the proposed IR-UWB receiver front-end.

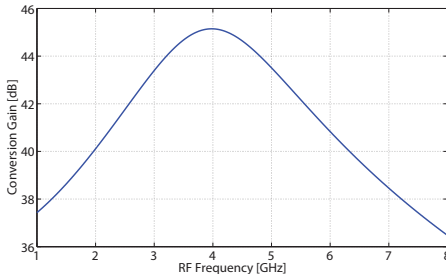


Fig. 6. The conversion gain in the highest gain mode.

simulation, and is competitive to other state-of-the-art IR-UWB receiver front-ends in CMOS.

#### ACKNOWLEDGMENT

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TABLE I  
COMPARISON WITH THE STATE OF THE ART

Design	[10]	[11]	[12]	This Work
CMOS technology	0.18 $\mu\text{m}$	90 nm	90 nm	90 nm
Die area ( $\text{mm}^2$ )	–	1.1	2.25	0.9
Power cons. (mW)	28.8	16.3	22.5	26.6
Conversion gain (dB)	25	0–18	6–45	35–45
-3 dB BW (GHz)	3–5	3–5	3–5	3–5
$S_{11}$ (dB)	$\leq -10$	$\leq -10$	$\leq -7.8$	$\leq -12$
NF (dB)	8	8.5	7.7–9.1	8–9
Sensitivity (dBm)	–	-89	-88	-89

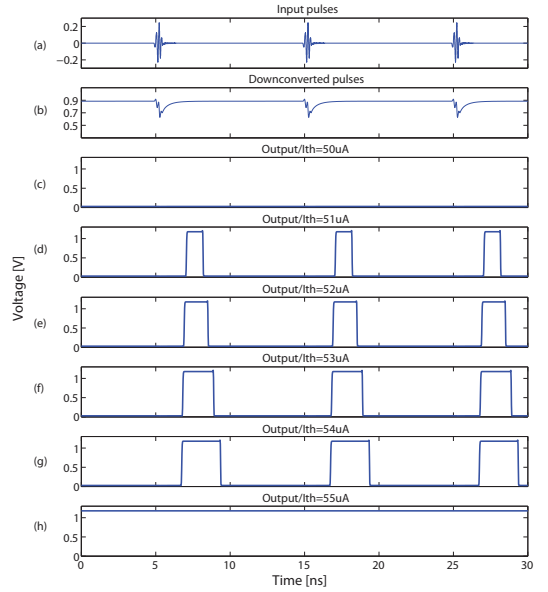


Fig. 7. The receiver performance when the threshold levels are swept.

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